(2)

FINAL TECHNICAL REPORT

FOR PERIOD FROM JANUARY 1991 THROUGH JULY 1992

Reference: NRL/SOHO Contract No. N00014-91-C-2052

SUMMARY: TOPICS COVERED IN THIS REPORT

1) FINAL SCHEDULE
2) SUMMARY of EXPENSES/BILLINGS (not final)
3) INDEX OF MONTHLY TECHNICAL REPORTS
4) INDEX OF QUALIFICATION TESTING REPORTS
5) LIST OF CCDs DELIVERED (LOTS 1, 2, 3, 4)
6) INDEX OF TECHNICAL PAPERS

The attached pages provide you with detailed information on these topics.

PREPARED BY:

Jon Ferrara

Jon Ferrara
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115 pg

1.0 FINAL SCHEDULE

Attached is a detailed Schedule for all work on the SOHO Program.

LOT #1 CCDs, by OCT. 14, 1991.
This task was COMPLETED on Nov. 7, 1991.

LOT #2 CCDs by NOV. 25, 1991.
This task was COMPLETED on Feb. 28, 1992.

LOT #3 CCDs.
This task was COMPLETED on May 7, 1992.

LOT #4 CCDs.
This task was COMPLETED on July 15, 1992.

2.0 SUMMARY of EXPENSES/BILLINGS

The first Billing occurred on 5-25-91 (Tek Accounting Period 113)

Billings for the current AP, and to date are as follows:

	Tektronix Accounting Period	Date	AP $	CUM $
(revised)	113	05-25-91	$168,831	$168,831
	201	06-29-91	$ 39,090	$207,921
	202	07-27-91	$ 41,242	$249,163
	203	08-24-91	$ 48,214	$297,377
	204	09-21-91	$ 55,269	$352,646
	205	10-19-91	$ 83,382	$436,027
	206	11-16-91	$ 65,284	$501,310
	207	12-14-91	$ 38,365	$539,677
	208	01-11-92	$ 23,449	$563,126
	209	02-08-92	$ 49,771	$612,897
	210	03-07-92	$ 43,695	$656,592
	211	04-04-92	$ 54,377	$710,969
	212	05-02-92	$ 30,432	$741,400
	213	05-30-92	$ 13,395	$754,795
	301	estimated	$ 20,000	
	302	estimated	$ 20,000	
	303	estimated	$ 10,000	

Statement A per telecon George Kowalski
NRL/Code 4167
Washington, DC 20375-5000

NWW 8/14/92

3.0 INDEX OF MONTHLY TECHNICAL REPORTS

Report Date: Month/Year (See attached copies)

1) January 7, 1991 through March 31, 1991 (first report)
2) April 1991
3) May 1991
4) June 1991
5) July 1991
6) August 1991
7) September 1991
8) October 1991
9) November 1991
10) December 1991
11) January 1992
12) February 1992
13) March 1992
14) April 1992
15) May 1992
16) June 1992
17) July 1992 (Final Technical Report)

4.0 INDEX OF QUALIFICATION TESTING REPORTS

Qualification testing was performed on two samples from each of Lots #1, 2, 3, 4. Attached are copies of the reports.

Report Title and Date:

1) SOHO Lot #1 Qualification Samples & Test Data Package, November 5, 1991.

2) SOHO Lot #2 Qualification Samples & Test Data Package, February 26, 1992.

3) SOHO Lot #3 Qualification Samples & Test Data Package, May 15, 1992.

4) SOHO Lot #4 Qualification Samples & Test Data Package, June 25, 1992.

5.0 LIST OF CCDs SHIPPED

1) Wafer Lot #1

Lot #1 comprises Deliverable Item Numbers 00108 and 00109.

Lot Number	Grade	Front/Back	Tek Part Number
1450AN07-01	Flight Candidate	Front	806-7735-56
1450AN11-01	Flight Candidate	Front	806-7735-56
1450AN12-01	Flight Candidate	Front	806-7735-56
1450AN11-02	Flight Candidate	Front	806-7735-56
1450AN19-04	Flight Candidate	Front	806-7735-56
1450AN11-03	Electrical Sample	Front	806-7735-57
1450AN11-04	Electrical Sample	Front	806-7735-57
1450AN12-02	Electrical Sample	Front	806-7735-57
1450AN13-04	Electrical Sample	Front	806-7735-57
1450AN19-03	Electrical Sample	Front	806-7735-57

2) Wafer Lot #2

Lot #2 comprises Deliverable Item Numbers 00110 and 00111.

Lot Number	Grade	Front/Back	Tek Part Number
1453AN02-01	Flight Candidate	Front	806-7735-56
1453AN02-04	Flight Candidate	Front	806-7735-56
1453AN04-02	Flight Candidate	Front	806-7735-56
1453AN05-02	Flight Candidate	Front	806-7735-56
1453AN05-03	Flight Candidate	Front	806-7735-56
1453AN04-01	Electrical Sample	Front	806-7735-57
1453AN05-01	Electrical Sample	Front	806-7735-57
1453AN02-03	Electrical Sample	Front	806-7735-57
1453BN06-02	Electrical Sample	Back	806-7735-77
1453CN11-02	Electrical Sample	Back	806-7735-77

3) Wafer Lot #3

Lot #3 comprises Deliverable Item Numbers 00110 and 00111.

Lot Number	Grade	Front/Back	Tek Part Number
1461BN19-04	Flight Candidate	Back	806-7735-76
1461BN15-02	Flight Candidate	Back	806-7735-76
1461BN19-02	Flight Candidate	Back	806-7735-76
1461AN01-01	Flight Candidate	Front	806-7735-56
1461AN03-01	Flight Candidate	Front	806-7735-56
1461AN04-03	Flight Candidate	Front	806-7735-77
1461AN01-04	Electrical Sample	Front	806-7735-57
1461AN02-03	Electrical Sample	Front	806-7735-57
1461AN02-04	Electrical Sample	Front	806-7735-57
1461AN03-04	Electrical Sample	Front	806-7735-57

5.0 LIST OF CCDs SHIPPED.....continued

4) Wafer Lot #4

Lot #4 comprises Deliverable Item Numbers 00114 and 00115.

Lot Number	Grade	Front/Back	Tek Part Number
1489AN03-01	Flight Candidate	Front	806-7735-56
1489AN03-02	Flight Candidate	Front	806-7735-56
1489AN04-04	Flight Candidate	Front	806-7735-56
1489AN05-02	Flight Candidate	Front	806-7735-56
1489AN10-04	Flight Candidate	Front	806-7735-56
1489AN04-03	Electrical Sample	Front	806-7735-57
1489AN10-02	Electrical Sample	Front	806-7735-57
1489AN20-01	Electrical Sample	Front	806-7735-57
1489CN13-02	Electrical Sample	Back	806-7735-77
1489CN19-04	Electrical Sample	Back	806-7735-77

6.0 INDEX OF TECHNICAL PAPERS

See attachments:

1. **Extreme UltraViolet Response of a Tektronix 1024 X 1024 CCD.** D. Moses, Naval Research Lab; J. F. Hochedez, University Space Research Association; R.A. Howard and B. Au, Naval Research Lab; D. Wang, Interferometrics, Inc.; M. M. Blouke, Tektronix, Inc.

2. **Charge Transfer Efficiency Measurements at Low Signal Levels on STIS/SOHO TK1024 CCD's.** J. D. Orbock, D. Murata-Seawalt, and W. A. Delamere, Ball Aerospace Systems Group; M. M. Blouke, Tektronix, Inc. Feb 1990, SPIE Proceedings Optical Sensors & CCDs.

APPENDIX

CONTENTS:

1) FINAL SCHEDULE

2) MONTHLY TECHNICAL REPORTS

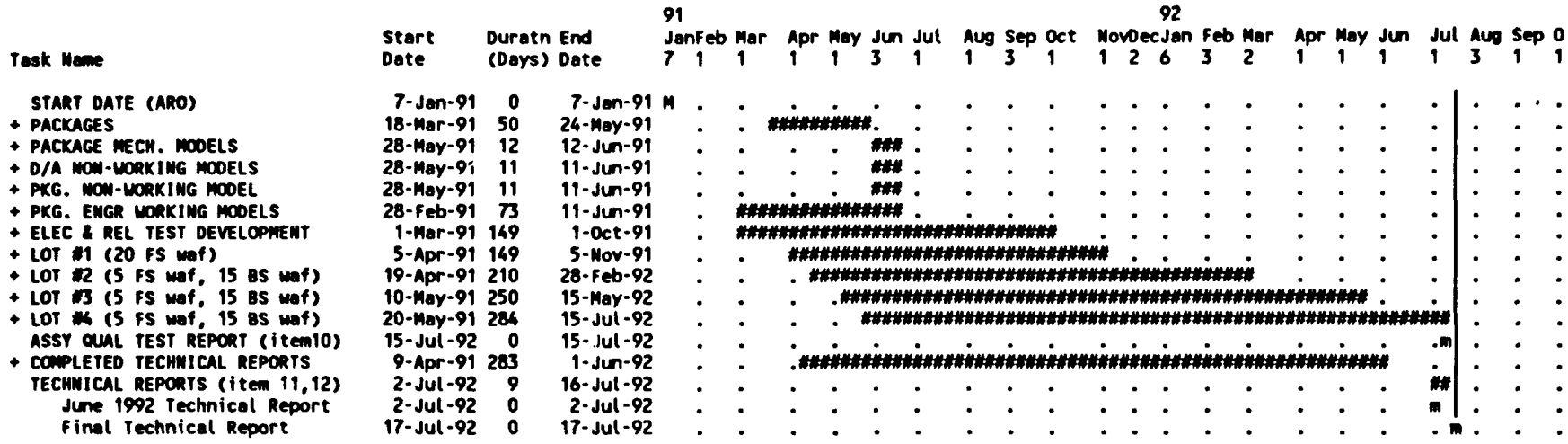
3) QUALIFICATION TESTING REPORTS

4) TECHNICAL PAPERS

FINAL SCHEDULE

Schedule Name : NRL/SOHO PROGRAM
Responsible : Jon Ferrara (Program Manager)
As-of Date : 17-Jul-92 8:00am Schedule File : A:\NRLSOHO

Monthly Status for Current/Planned Activities



XXXXX Detail Task ##### Summary Task M Milestone
xxxxx (Started) ==### (Started) >>> Conflict
XXX-- (Slack) ###-- (Slack) ..XXX Resource delay

---------- Scale: 1 week per character ----------

MONTHLY TECHNICAL REPORTS

Jon F.

PO Box 500
Beaverton, OR 97077
503-627-7111
Telex 192825 TEKTRONIX

Tektronix
COMMITTED TO EXCELLENCE

April 9, 1991

Mrs. Hilda Abdon
Naval Research Laboratory
Code 3240 (HA)
4555 Overlook Ave., SW
Washington, D.C. 20375-5000

Attention: Mrs. Hilda Abdon:

Reference: NRL/SOHO Contract No. N00014-91-C-2052

SUBJECT: Quarterly Technical Report & Program Schedule
For period from January 7, 1991 through March 31, 1991

SUMMARY: TOPICS COVERED IN THIS REPORT

1) SCHEDULE/CONTRACT/STATEMENT OF WORK

2) EXPENSES/BILLINGS

3) TECHNICAL

- PROGRESS DURING 1ST QUARTER 1991

- PLANS FOR 2ND QUARTER 1991

The attached pages provide you with detailed information on these topics.

Regards,

Jon Ferrara

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copies: Ben Au
Morley Blouke
Bruce Bradford
Russ Howard
George Kowalski
Art Luthi
Kay Stowers

1.0 SCHEDULE/CONTRACT/STATEMENT OF WORK

Attached is a detailed Schedule for all work on the SOHO Program. Delivery dates are consistent with the DELIVERABLES section of the Statement of Work.

Based on a letter of authorization from NRL, we began work on the SOHO contract on January 7, 1991.

During the past three months a number of people at Tektronix, and NRL have participated in developing the technical goals (CCD Specifications), Statement of Work (including DELIVERABLES), Costing and Contract preparation. At the time of this report the actual CPFF Contract is in the final stages of sign-off. I would like to personally thank all of you (too numerous to name) that participated.

2.0 EXPENSES/BILLINGS

Because the SOHO contract is not in place as of this date, no billings have been made. Based on the letter of authorization from NRL, we began work on the SOHO contract on January 7, 1991. The CPFF Contract is in the final stages of sign-off, and we anticipate Billing our labor, materials, and burden to date immediately after the contract is formally approved. This Billing is expected to occur during April 1991.

3.0 TECHNICAL

3.1 PROGRESS DURING 1ST QUARTER 1991

1) Kickoff Meeting for SOHO Program/Multi-Layer Ceramic Package

On Jan. 10, 1991, a SOHO Program Kickoff Meeting was held at Tektronix. Main topics for discussion were: Open contract issues (Statement of Work, and CCD specifications), Multi-Layer Ceramic (MLC) Package, CCD Wafer Fab Process characteristics/choosing implants, shipping container, transfer of test data.

Attendees from NRL/Analytyx were: Ben Au, Russ Howard, Tony Rizzo, John Slusarczyk, Laurie Ortolano.

Attendees from Tektronix were: Jon Ferrara, Morley Blouke, Rick German, Vidya Kale, Art Luthi, Brian Corrie, Larry Riley, Analene Waterman, Kay Stowers

2) Multi-Layer Ceramic (MLC) Package Design Review

On Feb. 8, 1991, a MLC Package Design Review was held at Tektronix. At this meeting were representatives from the MLC package vendor, Kyocera, NRL, Analytyx, and Tektronix. Discussed were detail design layouts for each layer of the MLC, MLC mechanical dimensions and tolerances, and the package procurement schedule. Each of the representatives were given detailed design issues, and a schedule for resolving these issues.

Attendees from NRL/Analytyx were: Ben Au, Russ Howard, Tony Rizzo, John Slusarczyk, Laurie Ortolano.

Attendees from Kyocera were: Matt Driscoll, Kaz Imuta

Attendees from Tektronix were: Jon Ferrara, Morley Blouke, Rick German, Linda Haney, Vidya Kale, Art Luthi, Brian Corrie, Larry Riley, Analene Waterman, Kay Stowers, Bob Jennings

3) Follow-up Meeting for MLC Package, and Testing Issues

On March, 1, 1991, a follow-up meeting for the MLC Package, and Testing Issues was held at Tektronix.

Attendees from NRL were: Ben Au, Russ Howard

Attendees from Tektronix were: Jon Ferrara, Larry Riley, Brian Corrie, Harry Marsh, Mark Nelson

4) Drawings for MLC Package

As required in the Statement of Work, Deliverables item #1, on March 27, 1991, the Final MLC Package Drawings were sent to Ben Au. These were Kycoera Dwg. No. SD-560-9453-100 Revision D, dated 3-14-91. This completed Deliverables item #1 requirement.

5) Delivery of MLC Package Mechanical Models

Since the design was finalized on March 8, 1991, Kyocera was given approval to proceed with the manufacturing phase of the MLC packages. They plan to manufacture 120 MLC packages, and deliver them by May 17, 1991. After arrival at Tektronix, they will be given an Incoming Quality Assurance (IQA) inspection, then transferred to the CCD Engineering/Packaging area.

6) Transfer of CCD Test Data

At the March 1, 1991 meeting at Tektronix, Russ Howard (NRL) brought two IDL tapes (containing an image from a TEK/STIS 1024 X 1024 CCD). Mark Nelson (Tektronix) converted these to a tape format compatible with our MicroVAX. It is planned to transfer from Tektronix to NRL, Flight CCD Imager data using this method.

7) Mechanical and Electrical Models of 1024 X 1024 CCDs

Scrap material from STIS Lot 1310 have been identified and segregated for building the mechanical samples for SOHO. These CCDs are awaiting delivery of the MLC package (due on 5-17-91).

Four good wafers from from STIS Lot 1310 have been identified and segregated for building the electrical models for SOHO. Two of these wafers were processed as frontside CCDs, and the remaining two as backside CCDs. These wafers have completed wafer fabrication, and have been tested. They are awaiting delivery of the MLC package (due on 5-17-91).

8) Documentation for Lots 1, 2, 3, 4 (1024 X 1024 CCDs)

During the first quarter, wafer fab documentation was completed to allow this material to be run in a standard manufacturing mode.

9) 1024 x 1024 CCD Mask Design for Lots 1, 2, 3, 4

During the first quarter we completed mask design changes for five layers to accommodate the temperature sensing diode required by NRL. The same temperature sensing diode shall be used for both frontside and backside CCDs.

10) Miscellaneous Packaging and Shipping Container Development

During the first quarter we completed most of the design, and brass board model for the MLC package shorting cover. Draft drawings and a sample will be available during the second quarter.

Also, during the March 1, 1991 meeting, the shipping container design was discussed with Ben Au and Russ Howard. Some preliminary engineering design has been done. The main design issue to be resolved is whether the shipping container will hold one or two CCDs. This work will continue during the second and third quarters.

3.2 PLANS FOR 2ND QUARTER 1991

1) Delivery of MLC Package Mechanical Models

The MLC packages being manufactured by Kycoera are due to be delivered to Tektronix by 5-17-91. After arrival at Tektronix, they will be given an Incoming Quality Assurance (IQA) inspection, then transferred to the CCD Engineering/Packaging area. They will be checked again by our package engineers, then the package mechanical models will be prepared for delivery and shipped to NRL by 5-31-91.

This will complete Deliverables item 2.

2) Delivery of Mechanical and Electrical Models

The scrap die from STIS Lot 1310 will be die attached, and wire bonded in the MLC package to prepare the mechanical model of the CCDs. These will be prepared for delivery and shipped to NRL by 6-14-91.

The four good wafers (two frontside and two backside) from STIS Lot 1310 will be sawed, die attached, wire bonded, and tested. These will be prepared for delivery to NRL by 6-14-91.

This will complete Deliverables items 3, 4, and 5.

3) Delivery of MLC Package Shorting Cover Model

Draft drawings and a brass board model of the MLC package shorting cover will be sent to NRL.

4) Start Wafer Fabrication for Lots 1 and 2

All wafer fabrication documentation will be put into place to start Deliverables Lots 1 and 2. Lot 1 will be started during April, and Lot 2 during May.

Note, delivery of CCDs from Lot 1 is due by Oct. 14, 1991, and delivery of CCDs from Lot 2 is due by Nov. 25, 1991.

5) Begin Electrical and Reliability Test Development

Begin development of the following electrical and reliability tests:

a) metal step coverage SEM test methods and documentation.
b) thermal cycling hardware and documentation.
c) shipping container drawings and models.
d) Keithley DC and Matrix test methods and documentation for wafer and package part testing.
e) AC test methods and documentation for wafer testing.
f) burn-in test hardware (burn-in boards) design, procurement, and documentation.
g) cold camera test hardware/software for interim and final test of the CCDs.

DELIVERABLES:

The deliverable items are based on a starting date of Jan. 7, 1991.

DELIVERABLES	DUE DATE
1. Drawings for custom ceramic package.	Apr. 1, 1991 (12 weeks ARO)
2. 2 package mechanical models which will be an initial sample of the custom ceramic package. They will closely resemble the final package and should be usable for mechanical setup.	May 31, 1991 (21 weeks ARO)
3. 2 packages and 5 packaged mechanical models with electrically failed CCD die attached for mechanical evaluation. One sample must be a thinned CCD die. The samples should be representative of the final package and die configuration.	Jun 14, 1991 (23 weeks ARO)
4. One qualification model with a non-working CCD mounted on the final package configuration. The model should be a mechanical representation of the final package with all bond wires, etc.	Jun 14, 1991 (23 weeks ARO)
5. The remaining two frontside and two backside wafers from the SOHO 1024 lot will completed and all working devices packaged. The devices will be screened and all devices that produce an image will be delivered. It is anticipated that this will give 9 engineering model devices with at least one backside device.	Jun 14, 1991 (23 weeks ARO)
6. At least 5 SOHO CCDs from Wafer Lot #1 (see Note 1), 5 electrical samples, and test data on all flight candidate devices.	Oct.14, 1991 (40 weeks ARO)
7. At least 5 SOHO CCDs from Wafer Lot #2 (see Note 1), 5 electrical samples, and test data on all flight candidate devices.	Nov.25, 1991 (46 weeks ARO)
8. At least 6 SOHO CCDs from Wafer Lot #3 (see Note 1), 5 electrical samples, and test data on all flight candidate devices.	Jan. 6, 1992 (52 weeks ARO)
9. At least 5 SOHO CCDs from Wafer Lot #4 (see Note 1), 5 electrical samples, and test data on all flight candidate devices.	Feb.17, 1992 (58 weeks ARO)
10. Report on assembly qualification tests.	Feb.17, 1992 (58 weeks ARO)
11. Quarterly Technical reports, and update of program schedule.	Quarterly
12. Final Technical Report.	Mar.17, 1992 (62 weeks ARO)

APRIL 1991 TECHNICAL REPORT & PROGRAM SCHEDULE

FOR PERIOD FROM APRIL 1, 1991 THROUGH APRIL 30, 1991

Reference: NRL/SOHO Contract No. N00014-91-C-2052

SUMMARY: TOPICS COVERED IN THIS REPORT

1) SCHEDULE/CONTRACT/STATEMENT OF WORK

2) EXPENSES/BILLINGS

3) TECHNICAL

- PROGRESS DURING APRIL 1991
- PLANS FOR MAY 1991

The attached pages provide you with detailed information on these topics.

PREPARED BY:

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1.0 SCHEDULE/CONTRACT/STATEMENT OF WORK

ALL ACTIVITIES ARE ON SCHEDULE.

Attached is a detailed Schedule for all work on the SOHO Program. Delivery dates are consistent with the DELIVERABLES section of the Statement of Work.

Based on a letter of authorization from NRL, we began work on the SOHO contract on January 7, 1991.

The contract was signed by Tektronix on April 17, 1991, and forwarded to Mrs. Hilda Abdon, NRL Subcontracts Manager.

2.0 EXPENSES/BILLINGS

Because the SOHO contract is not in place as of this date, no billings have been made. Based on the letter of authorization from NRL, we began work on the SOHO contract on January 7, 1991. The CPFF Contract is in the final stages of sign-off, and we anticipate Billing our labor, materials, and burden to date immediately after the contract is formally approved. This Billing is expected to occur during May 1991.

3.0 TECHNICAL

3.1 PROGRESS DURING APRIL 1991

1) <u>Delivery of MLC Package Mechanical Models</u>

Since the design was finalized on March 8, 1991, Kyocera was given approval to proceed with the manufacturing phase of the MLC packages. They plan to manufacture 120 MLC packages, and deliver them by May 17, 1991. After arrival at Tektronix, they will be given an Incoming Quality Assurance (IQA) inspection, then transferred to the CCD Engineering/Packaging area.

Kyocera has told us that they are still on schedule for delivery by 5-17-91. Also, Kyocera has requested a deviation to the pin diameter on their package drawing. Ben Au has been notified about this change, and is reviewing the deviation to the package drawing.

2) Transfer of CCD Test Data

At the March 1, 1991 meeting at Tektronix, Russ Howard (NRL) brought two IDL tapes (containing an image from a TEK/STIS 1024 X 1024 CCD). Mark Nelson (Tektronix) converted these to a tape format compatible with our MicroVAX. It is planned to transfer from Tektronix to NRL, Flight CCD Imager data using this method.

Since the 3-1-91 meeting, Tektronix has made hardware modifications to our tape drive which made it functional. We can now transfer data from the Photometrics Camera to the tape drive. During May, we plan to send some TK1024 images to Ben Au/Russ Howard in order to develop our data transfer method.

3) Mechanical and Electrical Models of 1024 X 1024 CCDs

Scrap material from STIS Lot 1310 have been identified and segregated for building the mechanical samples for SOHO. These CCDs are awaiting delivery of the MLC package (due on 5-17-91).

Four good wafers (thinned: wafers 2, 9; frontside wafers 10, 11) from from STIS Lot 1310 have been identified and segregated for building the electrical models for SOHO. Two of these wafers were processed as frontside CCDs, and the remaining two as backside CCDs. These wafers have completed wafer fabrication, and have been tested. They are awaiting delivery of the MLC package (due on 5-17-91).

4) Delivery of MLC Package Shorting Cover Model

Draft drawings and a brass board model of the MLC package shorting cover were sent to NRL (Ben Au) on 4-10-91. Ben is reviewing the adequacy of the design for use with Flight/electrical sample CCDs.

Because of the schedule for delivery of mechanical and electrical models by June 14, 1991, we are proceeding with present design for these CCDs.

5) Started Wafer Fabrication for Lots 1 and 2

Wafer Fabrication Lot #1 (#1450B) and Lot #2 (#1453B) were started on schedule.

Note, delivery of CCDs from Lot 1 is due by Oct. 14, 1991, and delivery of CCDs from Lot 2 is due by Nov. 25, 1991.

6) Started Documentation for Electrical and Reliability Tests.

Personnel assignments were made to begin developing and documenting the electrical and reliability test. The assembly drawing was completed, and the Flight Devices Test/Packaging Lot Traveler was prepared for signature approval.

3.2 PLANS FOR MAY 1991

1) Delivery of MLC Package Mechanical Models

The MLC packages being manufactured by Kycoera are due to be delivered to Tektronix by 5-17-91. After arrival at Tektronix, they will be given an Incoming Quality Assurance (IQA) inspection, then transferred to the CCD Engineering/Packaging area. They will be checked again by our package engineers, then the package mechanical models will be prepared for delivery and shipped to NRL by 5-31-91.

This will complete Deliverables item 2.

2) Delivery of Mechanical and Electrical Models

The scrap die from STIS Lot 1310 will be die attached, and wire bonded in the MLC package to prepare the mechanical model of the CCDs. These will be prepared for delivery and shipped to NRL by 6-14-91.

The four good wafers (thinned: wafers 2, 9; frontside wafers 10, 11) from from STIS Lot 1310 will begin assembly (die attach and wire bond) when the MLC packages arrive (due on 5-17-91). These will be tested and prepared for delivery to NRL by 6-14-91.

This will complete Deliverables items 3, 4, and 5.

3) Start Wafer Fabrication for Lot 3

Note, delivery of CCDs from Lot 3 is due by Nov. 22, 1991.

4) Begin Electrical and Reliability Test Development

Begin development of the following electrical and reliability tests:

a) metal step coverage SEM test methods and documentation.
b) thermal cycling hardware and documentation.
c) shipping container drawings and models.
d) Keithley DC and Matrix test methods and documentation for wafer and package part testing.
e) AC test methods and documentation for wafer testing.
f) burn-in test hardware (burn-in boards) design, procurement, and documentation.
g) cold camera test hardware/software for interim and final test of the CCDs.

5) Complete MLC Package Shorting Covers for Electrical Samples due for delivery by 6-14-91.

The existing design (sample sent to Ben Au on 4-10-91) is to be placed on order for manufacturing in Tek Bldg. 50 Machine Shop.

6) Transfer of CCD Test Data

Since the 3-1-91 meeting, Tektronix has made hardware modifications to our tape drive which made it functional. We can now transfer data from the Photometrics Camera to the tape drive. During May, we plan to send some TK1024 images to Ben Au/Russ Howard in order to develop our data transfer method.

MAY 1991 TECHNICAL REPORT & PROGRAM SCHEDULE

FOR PERIOD FROM MAY 1, 1991 THROUGH MAY 31, 1991

Reference: NRL/SOHO Contract No. N00014-91-C-2052

SUMMARY: TOPICS COVERED IN THIS REPORT

1) SCHEDULE/CONTRACT/STATEMENT OF WORK

2) EXPENSES/BILLINGS

3) TECHNICAL

- PROGRESS DURING MAY 1991
- PLANS FOR JUNE 1991

The attached pages provide you with detailed information on these topics.

PREPARED BY:

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1.0 SCHEDULE/CONTRACT/STATEMENT OF WORK

We have had some problems with shipment of delivery items due to processing and handling of the Federal Form DD250, Material Inspection and Receiving Report. This has caused delay of Deliverable Item Numbers 00101, and 00102.

Deliverable Item 00101, Drawings for custom ceramic package. This was originally completed on March 27, 1991 (Contract due date April 1, 1991). However, Form DD250 was not sent with these drawings. Therefore, during June 1991, I am planning to reship the drawings with the Form DD250.

Deliverable Item 00102, Two Package Models. The Contract due date was May 31, 1991. The packages were ready to ship on that date, but Form DD250 was not ready. Therefore, shipment was delayed while this paperwork was prepared. We plan to ship these by June 7, 1991.

Deliverable Items 00103, 00104, 00105, 00106, and 00107 are planned for shipment on schedule by June 14, 1991. These are as follows:

Item Number 00103:	Two custom ceramic packages.
Item Number 00104:	Four mechanical models with electrically failed CCD die attached.
Item Number 00105:	One mechanical model with thinned CCD die.
Item Number 00106:	One Qualification model with non-working CCD mounted with all bond wires.
Item Number 00107:	All remaining image producing package SOHO 1024 lot CCD devices.

ALL OTHER DELIVERABLE ITEMS ARE ON SCHEDULE.

Attached is a detailed Schedule for all work on the SOHO Program. Delivery dates are consistent with the DELIVERIES OR PERFORMANCE section of the Contract (PART I - SECTION F, page 7).

Based on a letter of authorization from NRL, we began work on the SOHO contract on January 7, 1991.

The contract was signed by Tektronix on April 17, 1991, and by the contracting officer for NRL (Ernest Tunney) on April 30, 1991. The Contract No. is: N00014-91C-2052.

2.0 EXPENSES/BILLINGS

The first Billing occurred on 5-22-91 (Tek Accounting Period 113)

Billings for the current AP, and to date are as follows:

Accounting Period	Date	AP $	CUM $
113	05-22-91	$76532	$76532

3.1 PROGRESS DURING MAY 1991

1) Delivery of MLC Package Mechanical Models

Since the design was finalized on March 8, 1991, Kyocera was given approval to proceed with the manufacturing phase of the MLC packages.

Kyocera completed manufacturing for 120 MLC packages, and delivered them on schedule on May 17, 1991. After arrival at Tektronix, these parts were given an Incoming Quality Assurance (IQA) inspection, and transferred to the CCD Engineering/Packaging area.

There was one problem with the pin diameter which occurred during manufacturing. However, prior to delivery to Tektronix, Kyocera reworked the parts to be within specification. A second problem occurred at Tektronix IQA, where the center mounting hole was measured to be smaller than the specification. A sample was sent back to Kyocera, and another sample pulled and remeasured at Tektronix. Both samples were found to be within specification. As a result, the 120 piece lot was accepted.

Two packages (serial no. 119, 120) were prepared for shipment to NRL, and are awaiting Form DD250. This will complete Deliverable Item 00102.

Two additional packages are being prepared for shipment to NRL (due date June 14, 1991) for Deliverable Item Number 00103.

2) Mechanical Models of 1024 X 1024 CCDs

Scrap material from STIS Lot 1310 has been identified and segregated for building the mechanical samples for SOHO. Packaging of this material was begun at the end of May when the packages from Kyocera arrived. There are 6 CCD die (all backside illuminated) which are being packaged.

These 6 CCD packaged die will be shipped as Deliverable Item Numbers 00104, 00105, and 00106.

3) Electrical Models of 1024 X 1024 CCDs

Four good wafers (thinned: wafers 2, 9; frontside wafers 10, 11) from STIS Lot 1310 were previously identified and segregated for building the electrical models for SOHO.

Die being packaged are from frontside wafers #10 and #11 have a total of 8 die, and backside wafer #2 has a total of 2 die remaining (backside wafer #9 was scrapped in fab). After packaging these parts will be given a functional test to verify they will produce and image and be shipped as Deliverable Item Number 00107.

3.1 PROGRESS DURING MAY 1991 (continued)

4) MLC Package Shorting Covers

Draft drawings and a brass board model of the MLC package shorting cover were sent to NRL (Ben Au) on 4-10-91. Ben is reviewing the adequacy of the design for use with Flight/electrical sample CCDs.

Because of the schedule for delivery of mechanical and electrical models by June 14, 1991, we are proceeding with present design for these CCDs.

Ten covers are being built in the Tektronix Model Shop, and are planned to be completed prior to June 14, 1991.

5) Wafer Lot #1

This lot (#1450B) is proceeding on schedule in frontside wafer fabrication, and is at Operation # 210. Deliverable Item Numbers 00108 and 00109 are due by Oct. 14, 1991.

6) Wafer Lot #2

This lot (#1453B) is proceeding on schedule in frontside wafer fabrication, and is at Operation # 117. Deliverable Item Numbers 00110 and 00111 are due by Nov. 25, 1991.

7) Wafer Lot #3

This lot was started on 5-16-91.

This lot (#1461B) is proceeding on schedule in frontside wafer fabrication, and is at Operation # 117. Deliverable Item Numbers 00112 and 00113 are due by Jan. 6, 1992.

8) Wafer Lot #4

This lot was started on 5-29-91.

This lot (#1464B) is proceeding on schedule in frontside wafer fabrication, and is at Operation # 117. Deliverable Item Numbers 00114 and 00115 are due by Feb. 17, 1992.

9) Started Documentation for Electrical and Reliability Tests.

Documentation and hardware development continued for the electrical and reliablity tests. The Test/Packaging Lot Traveler, DC Test, and Matrix/AC Test were completed. A probe card was ordered for the AC Test. The Camera Test hardware work was begun (cold finger, and head board changes). Also, Burn-in board design was begun.

3.1 PROGRESS DURING MAY 1991 (continued)

10) Transfer of CCD Test Data

During May we had planned to ship some TK1024 images to Ben Au/Russ Howard, but this activity was delayed due to time spent resolving the package procurement problems.

Since the 3-1-91 meeting, Tektronix has made hardware modifications to our tape drive which made it functional. We can now transfer data from the Photometrics Camera to the tape drive. During June, we plan to send some TK1024 images to Ben Au/Russ Howard in order to develop our data transfer method.

3.2 PLANS FOR JUNE 1991

1) Delivery of MLC Package Mechanical Models

Two packages (serial no. 119, 120) have been prepared for shipment to NRL, and are awaiting Form DD250. These are planned to be shipped to NRL by June 7, 1991. This will complete Deliverable Item 00102.

2) Delivery of Mechanical Models

Scrap material from STIS Lot 1310 has been identified and segregated for building the mechanical samples for SOHO. There are 6 CCD die (all backside illuminated) which are being packaged.

These 6 CCD packaged die will be shipped as Deliverable Item Numbers 00104, 00105, and 00106.

3) Delivery of Electrical Models

Four good wafers (thinned: wafers 2, 9; frontside wafers 10, 11) from STIS Lot 1310 were previously identified and segregated for building the electrical models for SOHO.

Die being packaged are from frontside wafers #10 and #11 have a total of 8 die, and backside wafer #2 has a total of 2 die remaining (backside wafer #9 was scrapped in fab).

After packaging these parts will be given a functional test to verify they will produce and image and be shipped as Deliverable Item Number 00107.

4) Complete MLC Package Shorting Covers for Electrical Samples due for delivery by 6-14-91.

The existing design (sample sent to Ben Au on 4-10-91) was placed on order for manufacturing in Tek Bldg. 50 Machine Shop, and is planned for completion by June 14, 1991.

3.2 PLANS FOR JUNE 1991 (continued)

5) Wafer Lot #1

Complete FS wafer fabrication. Select wafers for backside wafer fabrication.

6) Wafer Lot #2

Continue FS wafer fabrication.

7) Wafer Lot #3

Continue FS wafer fabrication.

8) Wafer Lot #4

Continue FS wafer fabrication.

9) Electrical and Reliability Test Development

Continue/complete development of the following electrical and reliability tests:

a) metal step coverage SEM test methods and documentation.
b) thermal cycling hardware and documentation.
c) shipping container drawings and models.
d) AC test hardware for wafer testing.
e) burn-in test hardware (burn-in boards) design, procurement, and documentation.
f) cold camera test hardware/software for interim and final test of the CCDs.

10) Transfer of CCD Test Data

Since the 3-1-91 meeting, Tektronix has made hardware modifications to our tape drive which made it functional. We can now transfer data from the Photometrics Camera to the tape drive. During June, we plan to send some TK1024 images to Ben Au/Russ Howard in order to develop our data transfer method.

11) Replacement Drawings for Deliverable Item 00101

Deliverable Item 00101, Drawings for custom ceramic package. This was originally completed on March 27, 1991 (Contract due date April 1, 1991). However, Form DD250 was not sent with these drawings. Therefore, during June 1991, I am planning to reship the drawings with the Form DD250.

JUNE 1991 TECHNICAL REPORT & PROGRAM SCHEDULE

FOR PERIOD FROM JUNE 1, 1991 THROUGH JUNE 30, 1991

Reference: NRL/SOHO Contract No. N00014-91-C-2052

SUMMARY: TOPICS COVERED IN THIS REPORT

1) SCHEDULE/CONTRACT/STATEMENT OF WORK

2) EXPENSES/BILLINGS

3) TECHNICAL

- PROGRESS DURING JUNE 1991
- PLANS FOR JULY 1991

The attached pages provide you with detailed information on these topics.

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1.0 SCHEDULE/CONTRACT/STATEMENT OF WORK

Attached is a detailed Schedule for all work on the SOHO Program. Delivery dates are consistent with the DELIVERIES OR PERFORMANCE section of the Contract No. N00014-91C-2052 (PART I - SECTION F, page 7).

NEXT MAJOR MILESTONE IS DELIVERY OF LOT #1 CCDs, by OCT. 4, 1991.

ALL REMAINING DELIVERABLE ITEMS ARE ON SCHEDULE.

2.0 EXPENSES/BILLINGS

The first Billing occurred on 5-22-91 (Tek Accounting Period 113)

Billings for the current AP, and to date are as follows:

Accounting Period	Date	AP $	CUM $
113	05-22-91	$76532	$ 76532
201	06-26-91	$92299	$168831
202			
203			
204			
205			
206			
207			
208			
209			
210			
211			
212			

3.0 TECHNICAL

3.1 PROGRESS DURING JUNE 1991

1) Delivery of MLC Package Mechanical Models

Since the design was finalized on March 8, 1991, Kyocera was given approval to proceed with the manufacturing phase of the MLC packages.

Kyocera completed manufacturing for 120 MLC packages, and delivered them on schedule on May 17, 1991. After arrival at Tektronix, these parts were given an Incoming Quality Assurance (IQA) inspection, and transferred to the CCD Engineering/Packaging area.

Two packages (serial no. 119, 120) were shipped to NRL on June 4, 1991. This completed Deliverable Item 00102.

Two additional packages (serial no. 017, 018) were shipped to NRL on June 17, 1991 (due date June 14, 1991). This completed Deliverable Item Number 00103.

3.1 PROGRESS DURING JUNE 1991 (continued)

2) Mechanical Models of 1024 X 1024 CCDs

Scrap material from STIS Lot 1310 was previously identified and segregated for building the mechanical samples for SOHO.

These 6 CCD packaged die were shipped to NRL on June 17, 1991 (due date June 14, 1991). This completed Deliverable Item Numbers 00104, 00105, and 00106.

3) Electrical Models of 1024 X 1024 CCDs

Four remaining wafers (thinned: wafers 2, 9; frontside wafers 10, 11) from STIS Lot 1310 were previously identified and segregated for building the electrical models for SOHO.

Eight die were packaged from frontside wafers #10 and #11, and two die were packaged from backside wafer #2 (backside wafer #9 was scrapped in fab). These 10 CCD electrical models (2 were non-functional) were shipped to NRL on June 17, 1991 (due date June 14, 1991).
This completed Deliverable Item Number 00107.

4) MLC Package Shorting Covers

Draft drawings and a brass board model of the MLC package shorting cover were sent to NRL (Ben Au) on 4-10-91. Ben is reviewing the adequacy of the design for use with Flight/electrical sample CCDs.

Eight covers were built in the Tektronix Model Shop, and used on the 8 functional electrical models (see item 3, above) which were shipped to NRL on June 17, 1991.

5) Wafer Lot #1

This lot (#1450B) is proceeding on schedule in frontside wafer fabrication, and is at Operation # 320. Deliverable Item Numbers 00108 and 00109 are due by Oct. 14, 1991.

This lot has been split between wafers with MPP implant, and wafers without MPP implant.

6) Wafer Lot #2

This lot (#1453B) is proceeding on schedule in frontside wafer fabrication, and is at Operation # 140. Deliverable Item Numbers 00110 and 00111 are due by Nov. 25, 1991.

3.1 PROGRESS DURING JUNE 1991 (continued)

7) Wafer Lot #3

This lot was started on 5-16-91.

This lot (#1461B) is proceeding on schedule in frontside wafer fabrication, and is at Operation # 140. Deliverable Item Numbers 00112 and 00113 are due by Jan. 6, 1992.

8) Wafer Lot #4

This lot was started on 5-29-91.

This lot (#1464B) is proceeding on schedule in frontside wafer fabrication, and is at Operation # 120. Deliverable Item Numbers 00114 and 00115 are due by Feb. 17, 1992.

9) Continued Documentation for Electrical and Reliability Tests

Documentation and hardware development continued for the electrical and reliablity tests. The Qualification Tests Lot Traveler, and Wire Bonding Diagrams were completed. A probe card was received for the AC Test. The Camera Test hardware work is continuing (cold finger, and head board changes).

On June 14, 1991 we FAXed the Burn-in board drawings to Ben Au for approval. This approval was received by FAX on June 19, 1991. Subsequently we completed the Burn-in board design, and ordered the Burn-in boards.

10) Transfer of CCD Test Data

On June 12, 1991 we shipped a magnetic tape with TK1024 images to Ben Au/Russ Howard in order to develop our data transfer method. We are awaiting feedback.

11) Replacement Drawings for Deliverable Item 00101

Deliverable Item 00101, Drawings for custom ceramic package. This was originally completed on March 27, 1991 (Contract due date April 1, 1991). However, Form DD250 was not sent with these drawings. Therefore, on June 4, 1991, these drawings were reshipped with Form DD250.

3.2 PLANS FOR JULY 1991

1) Review/Complete Design of MLC Package Shorting Covers for Flight Candidates/Electrical Samples

Engineering models of the final MLC package shorting cover were delivered on the Electrical Models shipped to NRL on June 14, 1991. We plan to review their acceptablity with Ben Au and complete the design during July.

2) Wafer Lot #1

Complete FS wafer fabrication.

3) Wafer Lot #2

Continue FS wafer fabrication.

4) Wafer Lot #3

Continue FS wafer fabrication.

5) Wafer Lot #4

Continue FS wafer fabrication.

6) Electrical and Reliability Test Development

Continue/complete development of the following electrical and reliability tests:

a) metal step coverage SEM test methods and documentation.
b) thermal cycling hardware and documentation.
c) shipping container drawings and models.
d) burn-in test hardware (burn-in boards) design, procurement, and documentation.
e) cold camera test hardware/software for interim, and final test of the CCDs.

7) Transfer of CCD Test Data

Review method which was used to ship TK1024 data to Ben Au and Russ Howard. (Magnetic tape sent June 12, 1991.)

8) Operation of TK1024 and M735A CCDs

Ben Au and Russ Howard plan to visit Tektronix on July 10 and July 11, 1991. One of the main purposes of this visit is to resolve voltage and clock settings needed to properly operate the TK1024 and M735A CCDs.

JULY 1991 TECHNICAL REPORT & PROGRAM SCHEDULE

FOR PERIOD FROM JULY 1, 1991 THROUGH JULY 31, 1991

Reference: NRL/SOHO Contract No. N00014-91-C-2052

SUMMARY: TOPICS COVERED IN THIS REPORT

1) SCHEDULE/CONTRACT/STATEMENT OF WORK

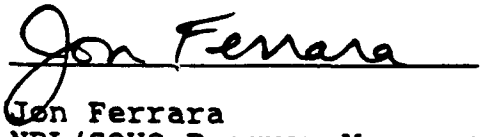
2) EXPENSES/BILLINGS

3) TECHNICAL

- PROGRESS DURING JULY 1991
- PLANS FOR AUGUST 1991

The attached pages provide you with detailed information on these topics.

PREPARED BY:



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1.0 SCHEDULE/CONTRACT/STATEMENT OF WORK

Attached is a detailed Schedule for all work on the SOHO Program. Delivery dates are consistent with the DELIVERIES OR PERFORMANCE section of the Contract No. N00014-91C-2052 (PART I - SECTION F, page 7).

NEXT MAJOR MILESTONE IS DELIVERY OF LOT #1 CCDs, by OCT. 14, 1991

ALL REMAINING DELIVERABLE ITEMS ARE ON SCHEDULE.

2.0 EXPENSES/BILLINGS

The first Billing occurred on 5-22-91 (Tek Accounting Period 113)

Billings for the current AP, and to date are as follows:

Accounting Period	Date	AP $	CUM $
113	05-22-91	$76532	$ 76532
201	06-26-91	$92299	$168831
202	07-22-91	$39090	$207921
203			
204			
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210			
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212			

3.0 TECHNICAL

3.1 PROGRESS DURING JULY 1991

1) Wafer Lot #1

This lot (#1450B) is proceeding on schedule in frontside wafer fabrication. Seven wafers completed wafer fabrication at the end of July, and the remaining ten wafers are expected out of wafer fabrication during the first week in August. Deliverable Item Numbers 00108 and 00109 are due by Oct. 14, 1991.

2) Wafer Lot #2

This lot (#1453B) is proceeding on schedule in frontside wafer fabrication, and is at Operation # 270. Deliverable Item Numbers 00110 and 00111 are due by Nov. 25, 1991.

3.1 PROGRESS DURING JULY 1991 (continued)

3) Wafer Lot #3

This lot (#1461B) is proceeding on schedule in frontside wafer fabrication, and is at Operation # 210. Deliverable Item Numbers 00112 and 00113 are due by Jan. 6, 1992.

4) Wafer Lot #4

This lot (#1464B) is proceeding on schedule in frontside wafer fabrication, and is at Operation # 140. Deliverable Item Numbers 00114 and 00115 are due by Feb. 17, 1992.

5) Continued Documentation for Electrical and Reliability Tests

Documentation and hardware development continued for the electrical and reliablity tests. The Camera Test hardware work is continuing (cold finger, and head board changes). The burn-in boards have been received, and are being assembled.

6) Meeting with Technical Leaders on 7-10-91 & 7-11-91.

On Wednesday/Thursday, 7-10-91 & 7-11-91, Morley Blouke and I met with program technical leaders (Ben Au & Russ Howard). The meeting was conducted at Tektronix for the purpose of discussing and resolving a number of technical issues as follows:

a) Review test data sent with NRL electrical sample CCDs.

Gary Spence explained all of the test data, photos, timing diagrams, and voltage/clock settings.

b) Review test data for loaned TK1024 frontside CCDs.

Ben Au returned these CCDs to Tektronix, and reviewed the data taken at NRL.

c) Loan a TK1024 backside CCD to NRL.

Ben Au signed a loan agreement for a backside TK1024 engineering grade, and hand carried this with him.

d) Demo the NRL electrical sample CCDs.

Gary Spence and Morley Blouke spent about one-half day demonstrating how to run these electrical samples.

e) Discuss modification to TK1DEV for NRL CCDs.

Ben Au, Russ Howard and Harry Marsh discussed modifications to TK1DEV in order to operate the M735A both frontside and backside. Tektronix plans to build two socketboards for this application.

3.1 PROGRESS DURING JULY 1991 (continued)

6) Meeting with Technical Leaders on 7-10-91 & 7-11-91. (cont.)

f) Discuss magnetic tape data transfer method.

Russ Howard reported that he was able to successfully read the TK1024 images previously sent to him on magnetic tape. It was agreed that this method was acceptable for shipping image data on flight candidate CCDs.

g) Review MLC package shorting cover design.

Rick German and Ben Au reviewed the design and construction of the MLC package shorting cover. It was agreed that the current design and construction was acceptable. Tektronix plans to order 50 production models of the shorting cover for use on deliverable items.

h) Deliver Documents for NRL Screening/Qualification Tests

Ben Au and Russ Howard requested copies of the screening and qualification tests which will be performed on the NRL CCDs. One copy of each were given to Ben/Russ during their visit. A new revision to these documents was subsequently delivered to Ben/Russ on 7-18-91.

i) SEM Tests for Front/Backside CCDs Step Coverage Screen.

Morley Blouke discussed with Ben Au/Russ Howard the methods used to perform the step coverage screen. It was agreed that SEM screens on frontside CCDs along with the test key data on step coverage test structures on backside wafers was adequate.

3.2 PLANS FOR AUGUST 1991

1) Wafer Lot #1

a) Complete FS wafer fabrication for remaining ten wafers.
b) Complete wafer testing (DC, Matrix, AC), select 20 best die for packaging.
c) Begin packaging.

2) Wafer Lot #2

Complete FS wafer fabrication.

3) Wafer Lot #3

Continue FS wafer fabrication.

4) Wafer Lot #4

Continue FS wafer fabrication.

5) Electrical and Reliability Test Development

Continue/complete development of the following electrical and reliability tests:

a) metal step coverage SEM test methods and documentation.
b) thermal cycling hardware and documentation.
c) shipping container drawings and models.
d) burn-in test hardware (burn-in boards) assembly, and documentation.
e) cold camera test hardware/software for interim, and final test of the CCDs.

AUGUST 1991 TECHNICAL REPORT & PROGRAM SCHEDULE

FOR PERIOD FROM AUGUST 1, 1991 THROUGH AUGUST 31, 1991

Reference: NRL/SOHO Contract No. N00014-91-C-2052

SUMMARY: TOPICS COVERED IN THIS REPORT

1) SCHEDULE/CONTRACT/STATEMENT OF WORK

2) EXPENSES/BILLINGS

3) TECHNICAL

- PROGRESS DURING AUGUST 1991
- PLANS FOR SEPTEMBER 1991

The attached pages provide you with detailed information on these topics.

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1.0 SCHEDULE/CONTRACT/STATEMENT OF WORK

Attached is a detailed Schedule for all work on the SOHO Program. Delivery dates are consistent with the DELIVERIES OR PERFORMANCE section of the Contract No. N00014-91C-2052 (PART I - SECTION F, page 7).

NEXT MAJOR MILESTONE IS DELIVERY OF LOT #1 CCDs, by OCT. 14, 1991

ALL REMAINING DELIVERABLE ITEMS ARE ON SCHEDULE.

2.0 EXPENSES/BILLINGS

The first Billing occurred on 5-25-91 (Tek Accounting Period 113)

Billings for the current AP, and to date are as follows:

	Accounting Period	Date	AP $	CUM $
(revised)	113	05-25-91	$168,831	$168,831
	201	06-29-91	$ 39,090	$207,921
	202	07-27-91	$ 41,242	$249,163
	203			
	204			
	205			
	206			
	207			
	208			
	209			
	210			
	211			
	212			

3.1 PROGRESS DURING AUGUST 1991

1) Wafer Lot #1

This lot (#1450B) is proceeding on schedule in frontside wafer fabrication. Seventeen wafers completed wafer fabrication at the beginning of August. Wafer testing was completed, 20 die were selected for packaging, and packaging was begun. Step coverage (SEM) screening was completed on test keys from two wafers. Deliverable Item Numbers 00108 and 00109 are due by Oct. 14, 1991.

2) Wafer Lot #2

This lot (#1453B) is proceeding on schedule in frontside wafer fabrication, and is at Operation # 340. Deliverable Item Numbers 00110 and 00111 are due by Nov. 25, 1991.

3) Wafer Lot #3

This lot (#1461B) is proceeding on schedule in frontside wafer fabrication, and is at Operation # 252. Deliverable Item Numbers 00112 and 00113 are due by Jan. 6, 1992.

4) Wafer Lot #4

This lot (#1464B) is proceeding on schedule in frontside wafer fabrication, and is at Operation # 210. Deliverable Item Numbers 00114 and 00115 are due by Feb. 17, 1992.

5) Continued Documentation for Electrical and Reliability Tests

Documentation and hardware development continued for the electrical and reliablity tests.

- The Camera Test hardware development and documentation was completed. We are awaiting the Lot #1 CCDs to checkout the Camera Test.
- The burn-in board hardware development and documentation was completed. We are awaiting Lot #1 CCDs to checkout the Burn-in Test.
- The Metal Step Coverage (SEM) Test was completed.

3.2 PLANS FOR SEPTEMBER 1991

1) Wafer Lot #1

a) Complete packaging.
b) Complete pre-burn-in Camera Test, Burn-in, post-burn-in Camera Test.
c) Begin Qualification Sample testing.

2) Wafer Lot #2

Complete FS wafer fabrication, and begin BS wafer fabrication.

3) Wafer Lot #3

Complete FS wafer fabrication.

4) Wafer Lot #4

Continue FS wafer fabrication.

5) Electrical and Reliability Test Development

Complete development of the following electrical and reliability tests:

b) thermal cycling hardware and documentation.
c) shipping container drawings and models.
d) burn-in test hardware/documentation checkout on Lot #1.
e) camera test hardware/software checkout on Lot #1.

SEPTEMBER 1991 TECHNICAL REPORT & PROGRAM SCHEDULE

FOR PERIOD FROM SEPTEMBER 1, 1991 THROUGH SEPTEMBER 30, 1991

Reference: NRL/SOHO Contract No. N00014-91-C-2052

SUMMARY: TOPICS COVERED IN THIS REPORT

1) SCHEDULE/CONTRACT/STATEMENT OF WORK

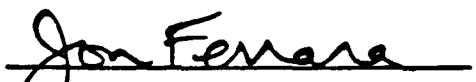
2) EXPENSES/BILLINGS

3) TECHNICAL

- PROGRESS DURING SEPTEMBER 1991
- PLANS FOR OCTOBER 1991

The attached pages provide you with detailed information on these topics.

PREPARED BY:



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1.0 SCHEDULE/CONTRACT/STATEMENT OF WORK

Attached is a detailed Schedule for all work on the SOHO Program. Delivery dates are consistent with the DELIVERIES OR PERFORMANCE section of the Contract No. N00014-91C-2052 (PART I - SECTION F, page 7).

- NEXT MAJOR MILESTONE FOR DELIVERY IS:

  LOT #1 CCDs, by OCT. 14, 1991. This task is currently running behind schedule by two weeks because of equipment downtime in packaging and wire bonding rework on these parts.

- REMAINING MAJOR MILESTONES FOR DELIVERY ARE:

  LOT #2 CCDs by NOV. 25, 1991. This task is currently running behind schedule by three weeks because of equipment downtime and capacity limitation in wafer fabrication.

  LOT #3 CCDs by JAN. 6, 1992. This task is currently running behind schedule by two weeks because of equipment downtime and capacity limitation in wafer fabrication.

  LOT #4 CCDs by FEB. 17, 1992. This task is currently running behind schedule by four weeks because of a wafer fabrication problem with this lot which required the material to be restarted on 10-4-91.

2.0 EXPENSES/BILLINGS

The first Billing occurred on 5-25-91 (Tek Accounting Period 113)

Billings for the current AP, and to date are as follows:

Accounting Period	Date	AP $	CUM $
(revised) 113	05-25-91	$168,831	$168,831
201	06-29-91	$ 39,090	$207,921
202	07-27-91	$ 41,242	$249,163
203	08-24-91	$ 48,214	$297,377
204	09-21-91	$ 54,603	$351,980
205			
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212			

3.1 PROGRESS DURING SEPTEMBER 1991

1) Wafer Lot #1

This lot (#1450B) completed frontside wafer fabrication at the beginning of August. During August, wafer testing was completed, 20 die selected for packaging, and packaging begun. During September packaging was completed, and 1st Camera Test was completed prior to Burn-In.

Deliverable Item Numbers 00108 and 00109 are due by Oct. 14, 1991. As noted on page 2 of this report, this task is currently running behind schedule by two weeks because of equipment downtime in packaging and wire bonding rework on these parts. The planned delivery schedule is Oct 29, 1991.

2) Wafer Lot #2

This lot (#1453B) completed frontside wafer fabrication (5 wafers only) at the beginning of September. During September, wafer testing was completed, 10 die selected for packaging, and packaging begun. The remaining 15 wafers were started into backside wafer fabrication.

Deliverable Item Numbers 00110 and 00111 are due by Nov. 25, 1991. As noted on page 2 of this report, this task is currently running behind schedule by three weeks because of equipment downtime and capacity limitation in wafer fabrication. The planned delivery schedule is Nov 12, 1991, and Dec. 12, 1991 for frontside and backside CCDs respectively.

3) Wafer Lot #3

This lot (#1461B) is continuing frontside wafer fabrication, and is at Operation # 340.

Deliverable Item Numbers 00112 and 00113 are due by Jan 6, 1992. As noted on page 2 of this report, this task is currently running behind schedule by two weeks because of equipment downtime and capacity limitation in wafer fabrication. The planned delivery schedule is Dec. 6, 1991, and Jan. 17, 1992 for frontside and backside CCDs respectively.

3.1 PROGRESS DURING SEPTEMBER 1991....continued

4) Wafer Lot #4

This lot (#1464B) was scrapped during frontside wafer fabrication on Oct. 4, 1991 because of a processing problem. The lot was restarted (#1489B).

Deliverable Item Numbers 00114 and 00115 are due by Feb. 17, 1992. As noted on page 2 of this report, this task is currently running behind schedule by four weeks. The planned delivery schedule is Feb. 3, 1992, and Mar. 16, 1992 for frontside and backside CCDs respectively.

5) Continued Documentation for Electrical and Reliability Tests

Documentation and hardware development continued for the electrical and reliablity tests.

- The Camera Test hardware/software and documentation was verified on Lot #1 CCDs.
- The burn-in board hardware and documentation is being verified on Lot #1 CCDs.
- The shipping container documentation was completed, and building of the hardware was started.
- The thermal cycling hardware and documentation was started.

3.2 PLANS FOR OCTOBER 1991

1) Wafer Lot #1

a) Complete Burn-in.
b) Complete post-burn-in Camera Test.
c) Complete Qualification Sample testing.
d) Complete shipment of Flight/Electrical CCDs.

2) Wafer Lot #2

a) Complete packaging, pre-burn-in Camera Test for frontside CCDs, Burn-in, and post-burn-in Camera Test.
b) Complete BS wafer fabrication.

3) Wafer Lot #3

a) Complete FS wafer fabrication, begin Wafer Test.
b) Begin BS wafer fabrication.

3.2 PLANS FOR OCTOBER 1991....continued

4) Wafer Lot #4

Continue FS wafer fabrication.

5) Electrical and Reliability Test Development

Complete development of the following electrical and reliability tests:

a) thermal cycling hardware and documentation verification on Lot #1.
b) shipping container hardware and drawing verification on Lot #1.

OCTOBER 1991 TECHNICAL REPORT & PROGRAM SCHEDULE

FOR PERIOD FROM OCTOBER 1, 1991 THROUGH OCTOBER 31, 1991

Reference: NRL/SOHO Contract No. N00014-91-C-2052

SUMMARY: TOPICS COVERED IN THIS REPORT

1) SCHEDULE/CONTRACT/STATEMENT OF WORK

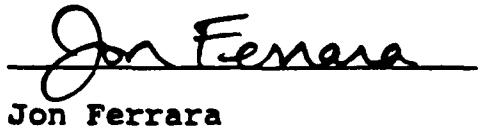
2) EXPENSES/BILLINGS

3) TECHNICAL

- PROGRESS DURING OCTOBER 1991
- PLANS FOR NOVEMBER 1991

The attached pages provide you with detailed information on these topics.

PREPARED BY:



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1.0 SCHEDULE/CONTRACT/STATEMENT OF WORK

Attached is a detailed Schedule for all work on the SOHO Program. Delivery dates are consistent with the DELIVERIES OR PERFORMANCE section of the Contract No. N00014-91C-2052 (PART I - SECTION F, page 7).

- NEXT MAJOR MILESTONE FOR DELIVERY IS:

LOT #1 CCDs, by OCT. 14, 1991. This task is currently running behind schedule by four weeks because of equipment downtime in packaging and wire bonding rework on these parts. In addition, the screen testing procedures (Camera tests before/after Burn-In) are taking longer than originally planned.

- REMAINING MAJOR MILESTONES FOR DELIVERY ARE:

LOT #2 CCDs by NOV. 25, 1991. This task is currently running behind schedule by seven weeks because of equipment downtime and capacity limitation in wafer fabrication. In addition, the screen testing procedures (Camera tests before/after Burn-In) are taking longer than originally planned.

LOT #3 CCDs by JAN. 6, 1992. This task is currently running behind schedule by seven weeks because of equipment downtime and capacity limitation in wafer fabrication. In addition, the screen testing procedures (Camera tests before/after Burn-In) are taking longer than originally planned.

LOT #4 CCDs by FEB. 17, 1992. This task is currently running behind schedule by eight weeks because of a wafer fabrication problem with this lot which required the material to be restarted on 10-4-91. In addition, the screen testing procedures (Camera tests before/after Burn-In) are taking longer than originally planned.

2.0 EXPENSES/BILLINGS

The first Billing occurred on 5-25-91 (Tek Accounting Period 113)

Billings for the current AP, and to date are as follows:

	Accounting Period	Date	AP $	CUM $
(revised)	113	05-25-91	$168,831	$168,831
	201	06-29-91	$ 39,090	$207,921
	202	07-27-91	$ 41,242	$249,163
	203	08-24-91	$ 48,214	$297,377
	204	09-21-91	$ 55,269	$352,646
	205	Not available as of 11-1-91.		
	206			
	207			
	208			
	209			
	210			
	211			
	212			

3.1 PROGRESS DURING OCTOBER 1991

1) Wafer Lot #1

This lot (#1450A) completed 160 hours of Burn-In and Final Camera testing during October. As of 11-1-91, the ten deliveribale CCDs (5 Flight Candidates, and 5 Electrical Samples) had been prepared for shipment to NRL and sent to the warehouse for delivery. They are now awaiting Form DD250 prior to shipment to NRL.

Deliverable Item Numbers 00108 and 00109 are due by Oct. 14, 1991. As noted on page 2 of this report, the completion of this task was delayed by about four weeks due to previous equipment downtime in packaging, wire bonding rework, and additional time required for Camera testing before/after Burn-In.

2) Wafer Lot #2

This lot (#1453) completed frontside wafer fabrication (5 wafers only) at the beginning of September. During October, ten die completed packaging, and Camera testing prior to Burn-In, and started into Burn-In on 11-1-91.

The remaining wafers completed backside wafer fabriciation (15 wafers started, 9 out) as of 11-1-91, and are at Wafer Test.

Deliverable Item Numbers 00110 and 00111 are due by Nov. 25, 1991. As noted on page 2 of this report, this task is currently running behind schedule by seven weeks because of equipment downtime and capacity limitation in wafer fabrication, and additional time required for Camera testing before/after Burn-In. The planned delivery schedule is Dec. 4, 1991, and Jan. 13, 1992 for frontside and backside CCDs respectively.

3) Wafer Lot #3

This lot (#1461) completed frontside wafer fabrication (5 wafers only) on 10-31-91, and are at Wafer Test.

The remaining wafers (15) have been strted into backside wafer fabrication.

Deliverable Item Numbers 00112 and 00113 are due by Jan 6, 1992. As noted on page 2 of this report, this task is currently running behind schedule by seven weeks because of equipment downtime and capacity limitation in wafer fabrication, and additional time required for Camera testing before/after Burn-In. The planned delivery schedule is Jan. 28, 1992, and Feb. 25, 1992 for frontside and backside CCDs respectively.

3.1 PROGRESS DURING OCTOBER 1991....continued

4) Wafer Lot #4

This lot (#1464B) was scrapped during frontside wafer fabrication on Oct. 4, 1991 because of a processing problem. The lot was restarted (#1489B), and is in wafer fabrication at Operation #117.

Deliverable Item Numbers 00114 and 00115 are due by Feb. 17, 1992. As noted on page 2 of this report, this task is currently running behind schedule by eight weeks. The planned delivery schedule is Mar. 2, 1992, and Apr. 13, 1992 for frontside and backside CCDs respectively.

5) Continued Documentation for Electrical and Reliability Tests

Documentation and hardware development continued for the electrical and reliablity tests.

- Completed verification of burn-in board hardware on Lot #1 CCDs.
- Completed building of shipping container hardware for Lot #1 CCDs.
- Sent shipping container drawings and cleaning procedures to Ben Au/Russ Howard for approval.
- The thermal cycling hardware was verified on Lot #1 CCDs.

3.2 PLANS FOR NOVEMBER 1991

1) Wafer Lot #1

a) Complete Qualification Sample testing.
b) Complete shipment of Flight/Electrical CCDs.

2) Wafer Lot #2

a) Complete Burn-in of FS CCDs.
b) Complete post-burn-in Camera Test for FS CCDs.
c) Complete Qualification Sample testing.
d) Complete Wafer Test, Packaging for BS CCDs.

3) Wafer Lot #3

a) Complete FS Wafer Test.
b) Complete FS packaging.
c) Continue BS wafer fabrication.

3.2 PLANS FOR NOVEMBER 1991....continued

4) Wafer Lot #4

Continue FS wafer fabrication.

5) Electrical and Reliability Test Development

Complete development of the following electrical and reliability tests:

a) Complete building of shipping containers for Lot #2.

NOVEMBER 1991 TECHNICAL REPORT & PROGRAM SCHEDULE

FOR PERIOD FROM NOVEMBER 1, 1991 THROUGH NOVEMBER 30, 1991

Reference: NRL/SOHO Contract No. N00014-91-C-2052

SUMMARY: TOPICS COVERED IN THIS REPORT

1) SCHEDULE/CONTRACT/STATEMENT OF WORK

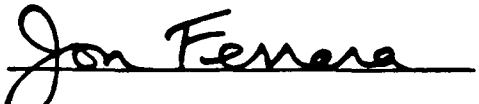
2) EXPENSES/BILLINGS

3) TECHNICAL

- PROGRESS DURING NOVEMBER 1991
- PLANS FOR DECEMBER 1991

The attached pages provide you with detailed information on these topics.

PREPARED BY:



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1.0 SCHEDULE/CONTRACT/STATEMENT OF WORK

Attached is a detailed Schedule for all work on the SOHO Program. Delivery dates are consistent with the DELIVERIES OR PERFORMANCE section of the Contract No. N00014-91C-2052 (PART I - SECTION F, page 7).

- FIRST LOT DELIVERY

  LOT #1 CCDs, by OCT. 14, 1991.
  This task was COMPLETED on Nov. 7, 1991.

- REMAINING LOTS FOR DELIVERY ARE:

  LOT #2 CCDs by NOV. 25, 1991. This task is currently running behind schedule by seven weeks because of equipment downtime and capacity limitation in wafer fabrication. In addition, the screen testing procedures (Camera tests before/after Burn-In) are taking longer than originally planned.

  LOT #3 CCDs by JAN. 6, 1992. This task is currently running behind schedule by seven weeks because of equipment downtime and capacity limitation in wafer fabrication. In addition, the screen testing procedures (Camera tests before/after Burn-In) are taking longer than originally planned.

  LOT #4 CCDs by FEB. 17, 1992. This task is currently running behind schedule by eight weeks because of a wafer fabrication problem with this lot which required the material to be restarted on 10-4-91. In addition, the screen testing procedures (Camera tests before/after Burn-In) are taking longer than originally planned.

2.0 EXPENSES/BILLINGS

The first Billing occurred on 5-25-91 (Tek Accounting Period 113)

Billings for the current AP, and to date are as follows:

	Accounting Period	Date	AP $	CUM $
(revised)	113	05-25-91	$168,831	$168,831
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	202	07-27-91	$ 41,242	$249,163
	203	08-24-91	$ 48,214	$297,377
	204	09-21-91	$ 55,269	$352,646
	205	10-19-91	$ 83,382	$436,027
	206	Not available as of 12-6-91.		
	207			
	208			
	209			
	210			
	211			
	212			

3.1 PROGRESS DURING NOVEMBER 1991

1) Wafer Lot #1

This lot (#1450A) completed shipment to NRL on 11-7-91. These were Deliverable Item Numbers 00108 and 00109.

2) Wafer Lot #2

This lot (#1453) completed frontside wafer fabrication (5 wafers only) at the beginning of September. During November, the frontside lot completed Burn-In, Post-Burn-In Camera Test, and shipment preparation. These frontside CCDs are currently ON HOLD awaiting completion of the backside CCDs, prior to shipment to NRL.

The remaining wafers completed backside wafer fabriciation (15 wafers started, 9 out) as of 11-1-91, and Wafer Test/Packaging during November. These backside CCDs are now being Camera tested prior to Burn-In.

On Nov. 27, 1992, two backside CCD electrical samples from Lot #2 were sent to NRL for evaluation. These were serial # 1453CN11-01, and 1453CN14-02.

Lot #2 comprises Deliverable Item Numbers 00110 and 00111.

3) Wafer Lot #3

This lot (#1461) completed frontside wafer fabrication (5 wafers only) on 10-31-91, and Wafer Test during November.

The remaining wafers (15) are continuing in backside wafer fabrication.

Lot #3 comprises Deliverable Item Numbers 00112 and 00113.

4) Wafer Lot #4

This lot (#1464B) was scrapped during frontside wafer fabrication on Oct. 4, 1991 because of a processing problem. The lot was restarted (#1489B), and is in continuing in frontside wafer fabrication.

Lot #4 comprises Deliverable Item Numbers 00114 and 00115.

5) Completed Shipping Hardware.

- Completed building of shipping container hardware for remaining Lots.

3.2 PLANS FOR DECEMBER 1991

1) Wafer Lot #2

   a) Complete Burn-in of BS CCDs.
   b) Begin post-burn-in Camera Test for BS CCDs.
   c) Complete Qualification Sample testing.
   d) Prepare for shipping FS/BS Flight Candidates and Electrical Samples by Jan. 28, 1992.

2) Wafer Lot #3

   a) Complete FS packaging.
   b) Continue BS wafer fabrication.

3) Wafer Lot #4

   Continue FS wafer fabrication.

DECEMBER 1991 TECHNICAL REPORT & PROGRAM SCHEDULE

FOR PERIOD FROM DECEMBER 1, 1991 THROUGH DECEMBER 31, 1991

Reference: NRL/SOHO Contract No. N00014-91-C-2052

SUMMARY: TOPICS COVERED IN THIS REPORT

1) SCHEDULE/CONTRACT/STATEMENT OF WORK

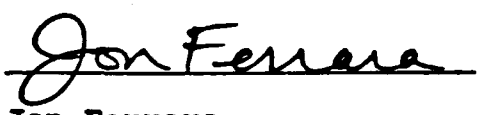
2) EXPENSES/BILLINGS

3) TECHNICAL

- PROGRESS DURING DECEMBER 1991
- PLANS FOR JANUARY 1992

The attached pages provide you with detailed information on these topics.

PREPARED BY:



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1.0 SCHEDULE/CONTRACT/STATEMENT OF WORK

Attached is a detailed Schedule for all work on the SOHO Program. Delivery dates are consistent with the DELIVERIES OR PERFORMANCE section of the Contract No. N00014-91C-2052 (PART I - SECTION F, page 7).

- FIRST LOT DELIVERY

  LOT #1 CCDs, by OCT. 14, 1991.
  This task was COMPLETED on Nov. 7, 1991.

- REMAINING LOTS FOR DELIVERY ARE:

  LOT #2 CCDs by NOV. 25, 1991. This task is currently running behind schedule by nine weeks because of equipment downtime and capacity limitation in wafer fabrication. In addition, the screen testing procedures (Camera tests before/after Burn-In) are taking longer than originally planned.

  LOT #3 CCDs by JAN. 6, 1992. This task is currently running behind schedule by seven weeks because of equipment downtime and capacity limitation in wafer fabrication. In addition, the screen testing procedures (Camera tests before/after Burn-In) are taking longer than originally planned.

  LOT #4 CCDs by FEB. 17, 1992. This task is currently running behind schedule by eight weeks because of a wafer fabrication problem with this lot which required the material to be restarted on 10-4-91. In addition, the screen testing procedures (Camera tests before/after Burn-In) are taking longer than originally planned.

2.0 EXPENSES/BILLINGS

The first Billing occurred on 5-25-91 (Tek Accounting Period 113)

Billings for the current AP, and to date are as follows:

	Tektronix Accounting Period	Date	AP $	CUM $
(revised)	113	05-25-91	$168,831	$168,831
	201	06-29-91	$ 39,090	$207,921
	202	07-27-91	$ 41,242	$249,163
	203	08-24-91	$ 48,214	$297,377
	204	09-21-91	$ 55,269	$352,646
	205	10-19-91	$ 83,382	$436,027
	206	11-16-91	$ 65,284	$501,310
	207	Not available as of 1-8-92.		
	208			
	209			
	210			
	211			
	212			

3.1 PROGRESS DURING DECEMBER 1991

1) Wafer Lot #1

This lot (#1450A) completed shipment to NRL on 11-7-91. These were Deliverable Item Numbers 00108 and 00109.

2) Wafer Lot #2

This lot (#1453) completed frontside wafer fabrication (5 wafers only) at the beginning of September. During December these frontside CCDs remained ON HOLD awaiting completion of the backside CCDs, prior to shipment to NRL.

During December, the backside CCDs completed Camera Test prior to burn-in, and Burn-In.

Also, during December, the two Qualification Samples were packaged, and prepared to begin qualification testing.

On Nov. 27, 1992, two backside CCD electrical samples from Lot #2 were sent to NRL for evaluation. These were serial # 1453CN11-01, and 1453CN14-02.

Lot #2 comprises Deliverable Item Numbers 00110 and 00111.

3) Wafer Lot #3

This lot (#1461) completed frontside wafer fabrication (5 wafers only) on 10-31-91, and Wafer Test during November. During December, 5 CCDs were packaged and are now ready for Camera Test prior to Burn-In.

One of the backside wafers (#11) completed wafer fab, packaging and test during December, and is awaiting Camera Test prior to burn-in. The remaining wafers (11) are continuing in backside wafer fabrication.

Lot #3 comprises Deliverable Item Numbers 00112 and 00113.

4) Wafer Lot #4

This lot (#1464B) was scrapped during frontside wafer fabrication on Oct. 4, 1991 because of a processing problem. The lot was restarted (#1489B), and is in continuing in frontside wafer fabrication.

Lot #4 comprises Deliverable Item Numbers 00114 and 00115.

5) Morley Blouke vist to NRL on Dec. 6, 1991

At the request of NRL, Morley Blouke traveled to NRL on 12-6-91 to discuss/advise NRL about the operation of the backside CCDs. The mission was successfully accomplished.

3.2 PLANS FOR JANUARY 1992

1) Wafer Lot #2

   a) Begin post-burn-in Camera Test for BS CCDs.
   b) Complete Qualification Sample testing.
   c) Prepare for shipping FS/BS Flight Candidates and Electrical Samples by Jan. 28, 1992.

2) Wafer Lot #3

   a) Complete FS Camera Test/Burn-In/Post Camera Test.
   b) Test/Package Additional FS CCDs.
   c) Complete BS wafer fabrication.
   d) Complete Camera Test prior to burn-in on CCDs from wafer #11.

3) Wafer Lot #4

   a) Complete FS wafer fabrication.
   b) Begin FS wafer testing.
   c) Begin BS wafer fabrication.

JANUARY 1992 TECHNICAL REPORT & PROGRAM SCHEDULE

FOR PERIOD FROM JANUARY 1, 1992 THROUGH JANUARY 31, 1992

Reference: NRL/SOHO Contract No. N00014-91-C-2052

SUMMARY: TOPICS COVERED IN THIS REPORT

1) SCHEDULE/CONTRACT/STATEMENT OF WORK

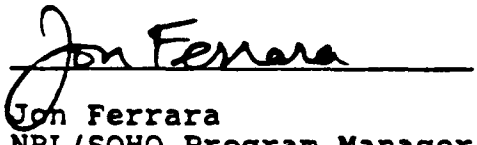
2) EXPENSES/BILLINGS

3) TECHNICAL

- PROGRESS DURING JANUARY 1992
- PLANS FOR FEBRUARY 1992

The attached pages provide you with detailed information on these topics.

PREPARED BY:



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1.0 SCHEDULE/CONTRACT/STATEMENT OF WORK

Attached is a detailed Schedule for all work on the SOHO Program. Delivery dates are consistent with the DELIVERIES OR PERFORMANCE section of the Contract No. N00014-91C-2052 (PART I - SECTION F, page 7).

- FIRST LOT DELIVERY

LOT #1 CCDs, by OCT. 14, 1991.
This task was COMPLETED on Nov. 7, 1991.

- REMAINING LOTS FOR DELIVERY ARE:

LOT #2 CCDs by NOV. 25, 1991. This task is currently running behind schedule, and planned for completion by Feb. 17, 1992.

The causes for the delay have been equipment downtime, capacity limitation in wafer fabrication, packaging/testing problems with backside CCDs, and yield problems with backside CCDs.

LOT #3 CCDs by JAN. 6, 1992. This task is currently running behind schedule, and planned for completion by May 19, 1992.

The causes for the delay are same as described above.

LOT #4 CCDs by FEB. 17, 1992. This task is currently running behind schedule, and planned for completion by June 30, 1992.

The causes for the delay are same as described above. In addition, because of a wafer fabrication problem with this lot, it was restarted on 10-4-91.

2.0 EXPENSES/BILLINGS

The first Billing occurred on 5-25-91 (Tek Accounting Period 113)

Billings for the current AP, and to date are as follows:

	Tektronix Accounting Period	Date	AP $	CUM $
(revised)	113	05-25-91	$168,831	$168,831
	201	06-29-91	$ 39,090	$207,921
	202	07-27-91	$ 41,242	$249,163
	203	08-24-91	$ 48,214	$297,377
	204	09-21-91	$ 55,269	$352,646
	205	10-19-91	$ 83,382	$436,027
	206	11-16-91	$ 65,284	$501,310
	207	12-14-91	$ 38,365	$539,677
	208	01-11-92	$ 23,449	$563,126
	209			
	210			
	211			
	212			

3.1 PROGRESS DURING JANUARY 1992

1) Wafer Lot #1

This lot (#1450A) completed shipment to NRL on 11-7-91. These were Deliverable Item Numbers 00108 and 00109.

2) Wafer Lot #2

This lot (#1453) completed frontside wafer fabrication (5 wafers only) at the beginning of September. During December these frontside CCDs remained ON HOLD awaiting completion of the backside CCDs, prior to shipment to NRL.

On Nov. 27, 1992, two backside CCD electrical samples from Lot #2 were sent to NRL for evaluation. These were serial # 1453CN11-01, and 1453CN14-02.

During January, the backside CCDs completed all of the required screening, and the two Qualification Samples completed qualification testing, and are ready for shipment.

Lot #2 CCDs are now ready for shipment to NRL pending review of the Camera test data by NRL. These CCDs are as follows:

Lot Number	Grade	Front/Back	Tek Part Number
1453AN05-02	Flight Candidate	Front	806-7735-56
1453AN05-03	Flight Candidate	Front	806-7735-56
1453AN02-01	Flight Candidate	Front	806-7735-56
1453AN02-03	Flight Candidate	Front	806-7735-56
1453AN02-04	Flight Candidate	Front	806-7735-56
1453AN04-01	Electrical Sample	Front	806-7735-57
1453AN05-01	Electrical Sample	Front	806-7735-57
1453BN06-02	Electrical Sample	Back	806-7735-77
1453CN11-02	Electrical Sample	Back	806-7735-77
1453CN19-02	Electrical Sample	Back	806-7735-77

Also, agreed upon during the teleconference, Tektronix shall proceed with modification to two of the backside process masks. This change is intended to improve the backside fabrication yields for Lot #3 and #4. This work will be charged to the contract project number 889159.

Lot #2 comprises Deliverable Item Numbers 00110 and 00111.

3.1 PROGRESS DURING JANUARY 1992....continued

3) Wafer Lot #3

This lot (#1461) completed frontside wafer fabrication (5 wafers only) on 10-31-91, and Wafer Test during November.

During January, all of the frontside CCDs completed screening and were placed on HOLD awaiting completion of the backside CCDs, prior to shipment to NRL.

During January, we determined this lot had backside yield problems, and wafer #11 was scrapped at Camera test. The remaining wafers (11) are continuing in backside wafer fabrication, and will use the two new backside process masks in order to improve their yield.

Lot #3 comprises Deliverable Item Numbers 00112 and 00113.

4) Wafer Lot #4

This lot (#1464B) was scrapped during frontside wafer fabrication on Oct. 4, 1991 because of a processing problem. The lot was restarted (#1489B), and is in continuing in frontside wafer fabrication.

Lot #4 comprises Deliverable Item Numbers 00114 and 00115.

3.2 PLANS FOR FEBRUARY 1992

1) Wafer Lot #2

a) Prepare for shipping FS/BS Flight Candidates and Electrical Samples by Feb. 17, 1992.

2) Wafer Lot #3

a) Continue to HOLD frontside CCDs for shipment.
b) Complete design/procurement of 2 new backside masks.
c) Continue BS wafer fabrication.

3) Wafer Lot #4

a) Complete FS wafer fabrication.
b) Begin FS wafer testing.
c) Begin BS wafer fabrication.

FEBRUARY 1992 TECHNICAL REPORT & PROGRAM SCHEDULE

FOR PERIOD FROM FEBRUARY 1, 1992 THROUGH FEBRUARY 29, 1992

Reference: NRL/SOHO Contract No. N00014-91-C-2052

SUMMARY: TOPICS COVERED IN THIS REPORT

1) SCHEDULE/CONTRACT/STATEMENT OF WORK

2) EXPENSES/BILLINGS

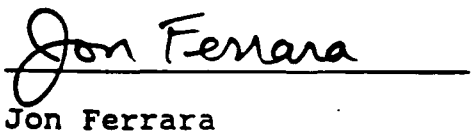
3) TECHNICAL

- PROGRESS DURING FEBRUARY 1992

- PLANS FOR MARCH 1992

The attached pages provide you with detailed information on these topics.

PREPARED BY:



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1.0 SCHEDULE/CONTRACT/STATEMENT OF WORK

Attached is a detailed Schedule for all work on the SOHO Program. Delivery dates are consistent with the DELIVERIES OR PERFORMANCE section of the Contract No. N00014-91C-2052 (PART I - SECTION F, page 7).

On Feb. 13, 1992, Kay Stowers, Tektronix Contract Administration, requested a no-cost extension to the contract completion date from Feb. 1992 to July 31, 1992.

- LOTS DELIVERED TO DATE:

  LOT #1 CCDs, by OCT. 14, 1991.
  This task was COMPLETED on Nov. 7, 1991.

  LOT #2 CCDs by NOV. 25, 1991.
  This task was COMPLETED on Feb. 28, 1992.

- REMAINING LOTS FOR DELIVERY ARE:

  LOT #3 CCDs by JAN. 6, 1992. This task is currently running behind schedule, and planned for completion by May 27, 1992.

  The causes for the delay have been equipment downtime, capacity limitation in wafer fabrication, packaging/testing problems with backside CCDs, and yield problems with back CCDs.

  LOT #4 CCDs by FEB. 17, 1992. This task is currently running behind schedule, and planned for completion by July 9, 1992.

  The causes for the delay are same as described above. In addition, because of a wafer fabrication problem with this lot, it was restarted on 10-4-91.

2.0 EXPENSES/BILLINGS

The first Billing occurred on 5-25-91 (Tek Accounting Period 113)

Billings for the current AP, and to date are as follows:

	Tektronix Accounting Period	Date	AP $	CUM $
(revised)	113	05-25-91	$168,831	$168,831
	201	06-29-91	$ 39,090	$207,921
	202	07-27-91	$ 41,242	$249,163
	203	08-24-91	$ 48,214	$297,377
	204	09-21-91	$ 55,269	$352,646
	205	10-19-91	$ 83,382	$436,027
	206	11-16-91	$ 65,284	$501,310
	207	12-14-91	$ 38,365	$539,677
	208	01-11-92	$ 23,449	$563,126
	209	02-08-92	$ 49,771	$612,897
	210	estimated	$ 60,000	
	211	estimated	$ 60,000	
	212	estimated	$ 60,000	
	213	estimated	$ 60,000	
	301	estimated	$ 60,000	
	302	estimated	$ 60,000	
	303 lump sum Fixed Fee.....		$ 88,000	

3.0 TECHNICAL

3.1 PROGRESS DURING FEBRUARY 1992

1) Wafer Lot #1

This lot (#1450A) completed shipment to NRL on 11-7-91. These were Deliverable Item Numbers 00108 and 00109.

2) Wafer Lot #2

This lot (#1453) completed backside screening and qualification during February. The Qualification Samples shipped to NRL were:

Lot No.	Pkg. Serial No.	Tek Part No.
1453AN02-02	050	806-7735-55 (frontside)
1453CN11-03	078	806-7735-75 (backside)

On 2-24-92, 5 Flight Candidates and 5 Electrical Samples were shipped to the Tektronix Government Warehouse awaiting the Form DD250. The Deliverable Item Number 00110 and 00111 were shipped to NRL on 2-28-92. These CCDs were as follows:

See next page.

3.1 PROGRESS DURING FEBRUARY 1992

2) Wafer Lot #2....continued

Lot Number	Grade	Front/Back	Tek Part Number
1453AN02-01	Flight Candidate	Front	806-7735-56
1453AN02-04	Flight Candidate	Front	806-7735-56
1453AN04-02	Flight Candidate	Front	806-7735-56
1453AN05-02	Flight Candidate	Front	806-7735-56
1453AN05-03	Flight Candidate	Front	806-7735-56
1453AN04-01	Electrical Sample	Front	806-7735-57
1453AN05-01	Electrical Sample	Front	806-7735-57
1453AN02-03	Electrical Sample	Front	806-7735-57
1453BN06-02	Electrical Sample	Back	806-7735-77
1453CN11-02	Electrical Sample	Back	806-7735-77

3) Wafer Lot #3

This lot (#1461) completed frontside wafer fabrication (5 wafers only) on 10-31-91, and Wafer Test during November.

During January, all of the frontside CCDs completed screening prior to burn-in. During February, 160 hour burn-in was completed on 12 frontside CCDs, and were placed on HOLD at Final Camera Test awaiting completion of the backside CCDs, prior to shipment to NRL.

During February, we completed the design and procurement of two new backside masks to improve yield.

During February 3 wafers completed backside wafer fabrication (could not use the new backside masks) and wafer test. The remaining wafers (8) are continuing in backside wafer fabrication, and will use the two new backside process masks in order to improve their yield.

Lot #3 comprises Deliverable Item Numbers 00112 and 00113.

4) Wafer Lot #4

This lot (#1464B) was scrapped during frontside wafer fabrication on Oct. 4, 1991 because of a processing problem. The lot was restarted (#1489B).

During February, this lot completed frontside wafer fabrication (wafers 3, 4, 5, 10, 20). The remaining wafers (14) continued on in backside processing (and will use the two new backside masks).

Lot #4 comprises Deliverable Item Numbers 00114 and 00115.

3.2 PLANS FOR MARCH 1992

1) Wafer Lot #3

   a) Complete screening for frontside CCDs (12).
   b) Complete BS wafer fabrication, and wafer testing.

2) Wafer Lot #4

   a) Complete FS wafer testing, and begin packaging.
   b) Continue BS wafer fabrication.

MARCH 1992 TECHNICAL REPORT & PROGRAM SCHEDULE

FOR PERIOD FROM MARCH 1, 1992 THROUGH MARCH 31, 1992

Reference: NRL/SOHO Contract No. N00014-91-C-2052

SUMMARY: TOPICS COVERED IN THIS REPORT

1) SCHEDULE/CONTRACT/STATEMENT OF WORK

2) EXPENSES/BILLINGS

3) TECHNICAL

- PROGRESS DURING MARCH 1992

- PLANS FOR APRIL 1992

The attached pages provide you with detailed information on these topics.

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1.0 SCHEDULE/CONTRACT/STATEMENT OF WORK

Attached is a detailed Schedule for all work on the SOHO Program. Delivery dates are consistent with the DELIVERIES OR PERFORMANCE section of the Contract No. N00014-91C-2052 (PART I - SECTION F, page 7).

On Feb. 13, 1992, Kay Stowers, Tektronix Contract Administration, requested a no-cost extension to the contract completion date from Feb. 1992 to July 31, 1992.

- LOTS DELIVERED TO DATE:

  LOT #1 CCDs, by OCT. 14, 1991.
  This task was COMPLETED on Nov. 7, 1991.

  LOT #2 CCDs by NOV. 25, 1991.
  This task was COMPLETED on Feb. 28, 1992.

- REMAINING LOTS FOR DELIVERY ARE:

  LOT #3 CCDs by JAN. 6, 1992. This task is currently running behind schedule, and planned for completion by May 12, 1992.

  The causes for the delay have been equipment downtime, capacity limitation in wafer fabrication, packaging/testing problems with backside CCDs, and yield problems with back CCDs.

  LOT #4 CCDs by FEB. 17, 1992. This task is currently running behind schedule, and planned for completion by June 30, 1992.

  The causes for the delay are same as described above. In addition, because of a wafer fabrication problem with this lot, it was restarted on 10-4-91.

2.0 EXPENSES/BILLINGS

The first Billing occurred on 5-25-91 (Tek Accounting Period 113)

Billings for the current AP, and to date are as follows:

	Tektronix Accounting Period	Date	AP $	CUM $
(revised)	113	05-25-91	$168,831	$168,831
	201	06-29-91	$ 39,090	$207,921
	202	07-27-91	$ 41,242	$249,163
	203	08-24-91	$ 48,214	$297,377
	204	09-21-91	$ 55,269	$352,646
	205	10-19-91	$ 83,382	$436,027
	206	11-16-91	$ 65,284	$501,310
	207	12-14-91	$ 38,365	$539,677
	208	01-11-92	$ 23,449	$563,126
	209	02-08-92	$ 49,771	$612,897
	210	03-07-92	$ 43,695	$656,592
	211	estimated	$ 60,000	
	212	estimated	$ 60,000	
	213	estimated	$ 60,000	
	301	estimated	$ 60,000	
	302	estimated	$ 60,000	
	303	lump sum Fixed Fee.....	$ 88,000	

3.0 TECHNICAL

3.1 PROGRESS DURING MARCH 1992

1) Wafer Lot #1

This lot (#1450A) completed shipment to NRL on 11-7-91. These were Deliverable Item Numbers 00108 and 00109.

2) Wafer Lot #2

This lot (#1453) completed shipment to NRL on 2-28-92. These were Deliverable Item Numbers 00110 and 00111.

3) Wafer Lot #3

This lot (#1461) completed frontside wafer fabrication (5 wafers only) on 10-31-91, and Wafer Test during November.

During January and February all of the frontside CCDs completed screening prior to burn-in, and 160 hour burnin. During March, 12 frontside CCDs completed Final Camera Test, Visual Inspection, and were placed on HOLD at Shipment Prep. awaiting completion of the backside CCDs, prior to shipment to NRL.

SEE NEXT PAGE

3) Wafer Lot #3 (continued)

These frontside CCDs are:

Lot Number	Part Number	Description
1461AN01-01	806-7735-56	FS Flight Candidate
1461AN01-03	"	" " "
1461AN02-01	"	" " "
1461AN03-01	"	" " "
1461AN03-03	"	" " "
1461AN04-01	"	" " "
1461AN05-02	"	" " "
1461AN05-04	"	" " "
1461AN01-04	806-7735-57	FS Electrical Sample
1461AN02-03	"	" " "
1461AN02-04	"	" " "
1461AN03-04	"	" " "

During February, 3 wafers (Lot 1461C, #8, 9, 12) completed backside wafer fabrication (could not use the new backside masks) and wafer test. During March, 8 wafers (Lot 1461B, #13,14,15,16,17,18,19,20) completed backside wafer fabrication, and wafer test. Note: These 8 wafers used the two new backside process masks in order to improve their yield. During March, 8 backside die completed packaging and Camera Test. After Camera Test, six backside die remained and were sent for Burn-In, these are:

Lot Number	Part Number	Description
1461CN09-01	806-7735-75	Ungraded BS CCD
1461BN15-02	"	" "
1461BN19-02	"	" "
1461BN19-03	"	" "
1461BN19-04	"	" "
1461BN20-02	"	" "

Lot #3 comprises Deliverable Item Numbers 00112 and 00113.

3.1 PROGRESS DURING MARCH 1992

4) Wafer Lot #4

This lot (#1464B) was scrapped during frontside wafer fabrication on Oct. 4, 1991 because of a processing problem. The lot was restarted (#1489B).

During February, this lot completed frontside wafer fabrication (Lot 1489A, wafers 3, 4, 5, 10, 20). During March, the frontside CCDs completed wafer testing, packaging, and are beginning Camera Test (prior to Burn-In). There were a total of 15 CCDs packaged, these are:

Lot Number	Part Number	Description
1489AN03-01	806-7735-55	FS Ungraded CCD
1489AN03-02	"	" "
1489AN03-03	"	" "
1489AN04-02	"	" "
1489AN04-03	"	" "
1489AN04-04	"	" "
1489AN05-01	"	" "
1489AN05-02	"	" "
1489AN05-03	"	" "
1489AN10-01	"	" "
1489AN10-02	"	" "
1489AN10-03	"	" "
1489AN10-04	"	" "
1489AN20-01	"	" "
1489AN20-02	"	" "

During March, the remaining 10 wafers (Lot 1489C, 7 wafers, Lot 1489B, 3 wafers) continued on in backside processing. Note: These 10 wafers used the two new backside process masks in order to improve their yield.

Lot #4 comprises Deliverable Item Numbers 00114 and 00115.

3.2 PLANS FOR APRIL 1992

1) Wafer Lot #3

a) Complete BS Burn-In, and Final Camera Test.
b) Complete FS/BS Qualification Testing.
c) Begin preparation for shipment of FS/BS CCDs.

2) Wafer Lot #4

a) Complete FS Burn-In, and Final Camera Test..
b) Complete BS wafer fabrication, and begin Wafer Test.

APRIL 1992 TECHNICAL REPORT & PROGRAM SCHEDULE

FOR PERIOD FROM APRIL 1, 1992 THROUGH APRIL 30, 1992

Reference: NRL/SOHO Contract No. N00014-91-C-2052

SUMMARY: TOPICS COVERED IN THIS REPORT

1) SCHEDULE/CONTRACT/STATEMENT OF WORK

2) EXPENSES/BILLINGS

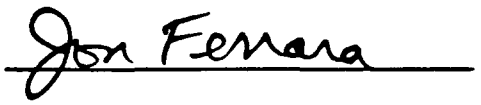
3) TECHNICAL

- PROGRESS DURING APRIL 1992

- PLANS FOR MAY 1992

The attached pages provide you with detailed information on these topics.

PREPARED BY:



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1.0 SCHEDULE/CONTRACT/STATEMENT OF WORK

Attached is a detailed Schedule for all work on the SOHO Program. Delivery dates are consistent with the DELIVERIES OR PERFORMANCE section of the Contract No. N00014-91C-2052 (PART I - SECTION F, page 7).

On Feb. 13, 1992, Kay Stowers, Tektronix Contract Administration, requested a no-cost extension to the contract completion date from Feb. 1992 to July 31, 1992.

- LOTS DELIVERED TO DATE:

  LOT #1 CCDs, by OCT. 14, 1991.
  This task was COMPLETED on Nov. 7, 1991.

  LOT #2 CCDs by NOV. 25, 1991.
  This task was COMPLETED on Feb. 28, 1992.

- REMAINING LOTS FOR DELIVERY ARE:

  LOT #3 CCDs.
  This task is currently planned for completion by May 15, 1992.

  LOT #4 CCDs.
  This task is currently planned for completion by July 15, 1992.

2.0 EXPENSES/BILLINGS

The first Billing occurred on 5-25-91 (Tek Accounting Period 113)

Billings for the current AP, and to date are as follows:

	Tektronix Accounting Period	Date	AP $	CUM $
(revised)	113	05-25-91	$168,831	$168,831
	201	06-29-91	$ 39,090	$207,921
	202	07-27-91	$ 41,242	$249,163
	203	08-24-91	$ 48,214	$297,377
	204	09-21-91	$ 55,269	$352,646
	205	10-19-91	$ 83,382	$436,027
	206	11-16-91	$ 65,284	$501,310
	207	12-14-91	$ 38,365	$539,677
	208	01-11-92	$ 23,449	$563,126
	209	02-08-92	$ 49,771	$612,897
	210	03-07-92	$ 43,695	$656,592
	211	04-04-92	$ 54,377	$710,969
	212	estimated	$ 60,000	
	213	estimated	$ 60,000	
	301	estimated	$ 60,000	
	302	estimated	$ 60,000	
	303	lump sum Fixed Fee.....	$ 88,000	

3.0 TECHNICAL

3.1 PROGRESS DURING APRIL 1992

1) Wafer Lot #1

This lot (#1450A) completed shipment to NRL on 11-7-91. These were Deliverable Item Numbers 00108 and 00109.

2) Wafer Lot #2

This lot (#1453) completed shipment to NRL on 2-28-92. These were Deliverable Item Numbers 00110 and 00111.

3) Wafer Lot #3

This is lot #1461. During April, this completed backside screening. The following frontside/backside CCDs completed screening, and are available for shipment. On 4-23-92, this list was FAXed to Ben Au and Russ Howard for selection of the CCDs to be shipped. On 4-29-92, Russ Howard selected the indicated (see "*") CCDs to be shipped. These are being placed in the proper shipping containers, a Certificate of Quality Conformance (C of QC) requested, and form DD 250 initiated.

CCDs available/selected for shipment are:

	Lot Number	Grade	Front/Back	Tek Part Number
*	1461BN19-04	Flight Candidate	Back	806-7735-76
	1461BN09-01	Electrical Sample	Back	806-7735-77
*	1461BN15-02	Flight Candidate	Back(see Note)	806-7735-76
*	1461BN19-02	Flight Candidate	Back(see Note)	806-7735-76
*	1461BN19-03	Electrical Sample	Back	806-7735-77
	1461BN20-02	Electrical Sample	Back	806-7735-77
*	1461AN01-01	Flight Candidate	Front	806-7735-56
	1461AN01-03	Flight Candidate	Front	806-7735-56
	1461AN02-01	Flight Candidate	Front	806-7735-56
*	1461AN03-01	Flight Candidate	Front	806-7735-56
	1461AN03-03	Flight Candidate	Front	806-7735-56
	1461AN04-01	Flight Candidate	Front	806-7735-56
*	1461AN04-03	Flight Candidate	Front	806-7735-56
	1461AN05-02	Flight Candidate	Front	806-7735-56
	1461AN05-04	Flight Candidate	Front	806-7735-56
*	1461AN01-04	Electrical Sample	Front	806-7735-57
*	1461AN02-03	Electrical Sample	Front	806-7735-57
*	1461AN02-04	Electrical Sample	Front	806-7735-57
*	1461AN03-04	Electrical Sample	Front	806-7735-57

NOTE: Upgraded from Electrical Sample to Flight Candidate by Russ Howard.

Lot #3 comprises Deliverable Item Numbers 00112 and 00113.

3.1 PROGRESS DURING APRIL 1992

4) Wafer Lot #4

This lot (#1464B) was scrapped during frontside wafer fabrication on Oct. 4, 1991 because of a processing problem. The lot was restarted (#1489B).

During February, this lot completed frontside wafer fabrication (Lot 1489A, wafers 3, 4, 5, 10, 20). During April all of the frontside CCDs completed screening. The frontside CCDs will be held until the backside CCDs have completed screening. The frontside CCDs available for shipment are:

Lot Number	Grade	Front/Back	Tek Part Number
1489AN03-01	Flight Candidate	Front	806-7735-56
1489AN03-02	Flight Candidate	Front	806-7735-56
1489AN10-02	Flight Candidate	Front	806-7735-56
1489AN10-04	Flight Candidate	Front	806-7735-56
1489AN04-03	Flight Candidate	Front	806-7735-56
1489AN04-04	Flight Candidate	Front	806-7735-56
1489AN05-02	Flight Candidate	Front	806-7735-56
1489AN05-03	Flight Candidate	Front	806-7735-56
1489AN20-02	Flight Candidate	Front	806-7735-56
1489AN20-01	Electrical Sample	Front	806-7735-57
1489AN03-03	Electrical Sample	Front	806-7735-57
1489AN04-02	Electrical Sample	Front	806-7735-57
1489AN10-01	Electrical Sample	Front	806-7735-57

During April, the lot was split with 1489C (6 wafers) completing backside processing onf 5-1-92. The remaining wafers (lot 1489B, 3 wafers) are still completing backside wafer fabrication.

Lot #4 comprises Deliverable Item Numbers 00114 and 00115.

3.2 PLANS FOR MAY 1992

1) Wafer Lot #3

a) Complete FS/BS Qualification Testing.
b) Complete shipment of FS/BS CCDs.

2) Wafer Lot #4

a) Complete BS wafer fabrication, complete BS Wafer Test, and begin BS Screening.

MAY 1992 TECHNICAL REPORT & PROGRAM SCHEDULE

FOR PERIOD FROM MAY 1, 1992 THROUGH MAY 31, 1992

Reference: NRL/SOHO Contract No. N00014-91-C-2052

SUMMARY: TOPICS COVERED IN THIS REPORT

1) SCHEDULE/CONTRACT/STATEMENT OF WORK

2) EXPENSES/BILLINGS

3) TECHNICAL

- PROGRESS DURING MAY 1992

- PLANS FOR JUNE 1992

The attached pages provide you with detailed information on these topics.

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1.0 SCHEDULE/CONTRACT/STATEMENT OF WORK

Attached is a detailed Schedule for all work on the SOHO Program. Delivery dates are consistent with the DELIVERIES OR PERFORMANCE section of the Contract No. N00014-91C-2052 (PART I - SECTION F, page 7).

On Feb. 13, 1992, Kay Stowers, Tektronix Contract Administration, requested a no-cost extension to the contract completion date from Feb. 1992 to July 31, 1992.

- LOTS DELIVERED TO DATE:

  LOT #1 CCDs, by OCT. 14, 1991.
  This task was COMPLETED on Nov. 7, 1991.

  LOT #2 CCDs by NOV. 25, 1991.
  This task was COMPLETED on Feb. 28, 1992.

  LOT #3 CCDs.
  This task was COMPLETED on May 7, 1992.

- REMAINING LOTS FOR DELIVERY ARE:

  LOT #4 CCDs.
  This task is currently planned for completion by July 15, 1992.

2.0 EXPENSES/BILLINGS

The first Billing occurred on 5-25-91 (Tek Accounting Period 113)

Billings for the current AP, and to date are as follows:

	Tektronix Accounting Period	Date	AP $	CUM $
(revised)	113	05-25-91	$168,831	$168,831
	201	06-29-91	$ 39,090	$207,921
	202	07-27-91	$ 41,242	$249,163
	203	08-24-91	$ 48,214	$297,377
	204	09-21-91	$ 55,269	$352,646
	205	10-19-91	$ 83,382	$436,027
	206	11-16-91	$ 65,284	$501,310
	207	12-14-91	$ 38,365	$539,677
	208	01-11-92	$ 23,449	$563,126
	209	02-08-92	$ 49,771	$612,897
	210	03-07-92	$ 43,695	$656,592
	211	04-04-92	$ 54,377	$710,969
	212	05-02-92	$ 30,432	$741,400
	213	estimated	$ 60,000	
	301	estimated	$ 60,000	
	302	estimated	$ 60,000	
	303 lump sum Fixed Fee.....		$ 88,000	

3.0 TECHNICAL

3.1 PROGRESS DURING MAY 1992

1) Wafer Lot #1

This lot (#1450A) completed shipment to NRL on 11-7-91. These were Deliverable Item Numbers 00108 and 00109.

2) Wafer Lot #2

This lot (#1453) completed shipment to NRL on 2-28-92. These were Deliverable Item Numbers 00110 and 00111.

3) Wafer Lot #3

This lot #1461 completed shipment to NRL on 5-7-92. These were Deliverable Item Numbers 00112 and 00113.

CCDs selected by NRL for shipment were:

Lot Number	Grade	Front/Back	Tek Part Number
1461BN19-04	Flight Candidate	Back	806-7735-76
1461BN15-02	Flight Candidate	Back(see Note)	806-7735-76
1461BN19-02	Flight Candidate	Back(see Note)	806-7735-76
1461BN19-03	Electrical Sample	Back	806-7735-77
1461AN01-01	Flight Candidate	Front	806-7735-56
1461AN03-01	Flight Candidate	Front	806-7735-56
1461AN04-03	Flight Candidate	Front	806-7735-56
1461AN01-04	Electrical Sample	Front	806-7735-57
1461AN02-03	Electrical Sample	Front	806-7735-57
1461AN02-04	Electrical Sample	Front	806-7735-57
1461AN03-04	Electrical Sample	Front	806-7735-57

NOTE: Upgraded from Electrical Sample to Flight Candidate by Russ Howard.

On May 15, 1992 the Lot #3 Qualification Samples (Lot Numbers 1461AN05-04 and 1461CN09-01) and Test Data were shipped to NRL. This completed all delivery items for this contract task.

3.1 PROGRESS DURING MAY 1992

4) Wafer Lot #4

This lot (#1464B) was scrapped during frontside wafer fabrication on Oct. 4, 1991 because of a processing problem. The lot was restarted (#1489B).

The frontside CCDs are being held until the backside CCDs have completed screening. The frontside CCDs available for shipment are:

Lot Number	Grade	Front/Back	Tek Part Number
1489AN03-01	Flight Candidate	Front	806-7735-56
1489AN03-02	Flight Candidate	Front	806-7735-56
1489AN10-02	Flight Candidate	Front	806-7735-56
1489AN10-04	Flight Candidate	Front	806-7735-56
1489AN04-03	Flight Candidate	Front	806-7735-56
1489AN04-04	Flight Candidate	Front	806-7735-56
1489AN05-02	Flight Candidate	Front	806-7735-56
1489AN05-03	Flight Candidate	Front	806-7735-56
1489AN20-02	Flight Candidate	Front	806-7735-56
1489AN20-01	Electrical Sample	Front	806-7735-57
1489AN03-03	Electrical Sample	Front	806-7735-57
1489AN04-02	Electrical Sample	Front	806-7735-57
1489AN10-01	Electrical Sample	Front	806-7735-57

During April, the lot was split with 1489C (6 wafers) completing backside processing onf 5-1-92. The remaining wafers (lot 1489B, 3 wafers) are still completing backside wafer fabrication.

Due to losses at Saw for wafer bow, and test/packaging yield, only 4 backside wafers from lot 1489C were packaged, as follows:

Lot Number	Wafer Number	Quantity
1489CN07	7	2
1489CN12	12	3
1489CN13	13	2
1489CN19	19	2

Lot #4 comprises Deliverable Item Numbers 00114 and 00115.

3.2 PLANS FOR JUNE 1992

1) Wafer Lot #4

a) Continue BS Screening.

b) Continue BS Qualification Sample testing.

JUNE 1992 TECHNICAL REPORT & PROGRAM SCHEDULE

FOR PERIOD FROM JUNE 1, 1992 THROUGH JUNE 30, 1992

Reference: NRL/SOHO Contract No. N00014-91-C-2052

SUMMARY: TOPICS COVERED IN THIS REPORT

1) SCHEDULE/CONTRACT/STATEMENT OF WORK

2) EXPENSES/BILLINGS

3) TECHNICAL

- PROGRESS DURING JUNE 1992

- PLANS FOR JULY 1992

The attached pages provide you with detailed information on these topics.

PREPARED BY:

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1.0 SCHEDULE/CONTRACT/STATEMENT OF WORK

Attached is a detailed Schedule for all work on the SOHO Program. Delivery dates are consistent with the DELIVERIES OR PERFORMANCE section of the Contract No. N00014-91C-2052 (PART I - SECTION F, page 7).

On Feb. 13, 1992, Kay Stowers, Tektronix Contract Administration, requested a no-cost extension to the contract completion date from Feb. 1992 to July 31, 1992.

- LOTS DELIVERED TO DATE:

  LOT #1 CCDs, by OCT. 14, 1991.
  This task was COMPLETED on Nov. 7, 1991.

  LOT #2 CCDs by NOV. 25, 1991.
  This task was COMPLETED on Feb. 28, 1992.

  LOT #3 CCDs.
  This task was COMPLETED on May 7, 1992.

- REMAINING LOTS FOR DELIVERY ARE:

  LOT #4 CCDs.
  This task is currently planned for completion by July 15, 1992.

2.0 EXPENSES/BILLINGS

The first Billing occurred on 5-25-91 (Tek Accounting Period 113)

Billings for the current AP, and to date are as follows:

	Tektronix Accounting Period	Date	AP $	CUM $
(revised)	113	05-25-91	$168,831	$168,831
	201	06-29-91	$ 39,090	$207,921
	202	07-27-91	$ 41,242	$249,163
	203	08-24-91	$ 48,214	$297,377
	204	09-21-91	$ 55,269	$352,646
	205	10-19-91	$ 83,382	$436,027
	206	11-16-91	$ 65,284	$501,310
	207	12-14-91	$ 38,365	$539,677
	208	01-11-92	$ 23,449	$563,126
	209	02-08-92	$ 49,771	$612,897
	210	03-07-92	$ 43,695	$656,592
	211	04-04-92	$ 54,377	$710,969
	212	05-02-92	$ 30,432	$741,400
	213	05-30-92	$ 13,395	$754,795
	301	estimated	$ 20,000	
	302	estimated	$ 20,000	
	303	estimated	$ 10,000	

3.0 TECHNICAL

3.1 PROGRESS DURING JUNE 1992

1) Wafer Lot #1

This lot (#1450A) completed shipment to NRL on 11-7-91. These were Deliverable Item Numbers 00108 and 00109.

2) Wafer Lot #2

This lot (#1453) completed shipment to NRL on 2-28-92. These were Deliverable Item Numbers 00110 and 00111.

3) Wafer Lot #3

This lot (#1461) completed shipment to NRL on 5-7-92. These were Deliverable Item Numbers 00112 and 00113.

4) Wafer Lot #4

This lot (#1464B) was scrapped during frontside wafer fabrication on Oct. 4, 1991 because of a processing problem. The lot was restarted (#1489B). Screening has been completed, and the following CCDs are being prepared for shipment:

Lot Number	Grade	Front/Back	Tek Part Number
1489AN03-01	Flight Candidate	Front	806-7735-56
1489AN03-02	Flight Candidate	Front	806-7735-56
1489AN04-04	Flight Candidate	Front	806-7735-56
1489[illegible]05-02	Flight Candidate	Front	806-7735-56
1489A[illegible]-04	Flight Candidate	Front	806-7735-56
1489AN04-03	Electrical Sample	Front	806-7735-57
1489AN10-02	Electrical Sample	Front	806-7735-57
1489AN20-01	Electrical Sample	Front	806-7735-57
1489CN13-02	Electrical Sample	Back	806-7735-77
1489CN19-04	Electrical Sample	Back	806-7735-77

Lot #4 comprises Deliverable Item Numbers 00114 and 00115.

Also, during June, the Lot #4 Qualification Sample testing was completed. These CCDs and test data were shipped to NRL on June 25th as follows:

Lot No.	Pkg. Serial No.	Tek Part No.
1489AN03-03	101	806-7735-55 (frontside)
1489CN12-01	032	806-7735-75 (backside)

3.2 PLANS FOR JULY 1992

1) Wafer Lot #4

   a) Ship Lot #4 CCDs.

   b) Complete Final Technical Report.

   c) Ship remaining CCDs to NRL.

QUALIFICATION TESTING REPORTS

Tektronix
COMMITTED TO EXCELLENCE

Tektronix, Inc.
Howard Vollum Park
P.O. Box 500
Beaverton, Oregon 97077-0001

Phone: (503) 627-7111

November 5, 1991

Mr. George Kowlaski
Naval Research Laboratory
4555 Overlook Ave., SW
Bldg. 209, Room 138
Washington, D.C. 20375-5000

Contract Number: N00014-91-C-2052
Code: 4167

ATTENTION: George Kowalski

SUBJECT: SOHO LOT #1 QUALIFICATION SAMPLES & TEST DATA PACKAGE

We have successfully completed the Qualification Testing on the CCD samples from SOHO Lot #1. Please note that these Qualification Samples PASSED all of the required tests as follows:

1. Thermal Cycle (-55 to +125C, 25 cycles): No visual defects.

2. 100% Destructive Wire Bond Pull Strength.

   Both parts had a mean and std. deviation of about 8 grams and 1 gram respectively. (Acceptable is greater than 2.5 grams.)

3. Die Shear Strength Test.

   Both parts passed with greater than 10 kilograms die shear strength. (Acceptable is greater than 0.75 kilogram.)

Enclosed are the Qualification Samples, and Test Data Package (3 copies) for SOHO Lot #1. The identification for these Qualification Samples is as follows:

Lot No.	Pkg. Serial No.	Tek Part No.
1450FN02-03	021	806-7735-55
1450AN07-02	023	806-7735-55

Please give these samples and data to Ben Au and Russ Howard. If you have any further questions regarding these Deliverable Items, then please contact me immediately.

Regards,

Jon Ferrara

Jon Ferrara
NRL/SOHO Program Manager
ICO/CCD Products

Tektronix, Inc.
P.O. Box 500
Mail Stop 59-567
Beaverton, Oregon 97077
(503) 627-6865

copies: Morley Blouke, Rick German

Tektronix
COMMITTED TO EXCELLENCE

Tektronix, Inc.
Howard Vollum Park
P.O. Box 500
Beaverton, Oregon 97077-0001

Phone: (503) 627-7111

February 26, 1992

Mr. George Kowlaski
Naval Research Laboratory
4555 Overlook Ave., SW
Bldg. 209, Room 138
Washington, D.C. 20375-5000

Contract Number: N00014-91-C-2052
Code: 4167

ATTENTION: Mr. George Kowalski

SUBJECT: SOHO LOT #2 QUALIFICATION SAMPLES & TEST DATA PACKAGE

We have successfully completed the Qualification Testing on the CCD samples from SOHO Lot #2. Please note that these Qualification Samples PASSED all of the required tests as follows:

1. Thermal Cycle (-55 to +125C, 25 cycles): No visual defects.

2. 100% Destructive Wire Bond Pull Strength.
   - Lot No. 1453AN02-02 had a mean and std. deviation of 12.3 grams, and 2.0 grams, respectively.
   - Lot No. 1453CN11-03 had a mean and std. deviation of 8.6 grams, and 1.8 grams. respectively.

Note: Acceptable wire bond pull strength is greater than 2.5 grams.

3. Die Shear Strength Test.
   Both parts passed with greater than 10 kilograms die shear strength. (Acceptable is greater than 0.75 kilogram.)

Enclosed are the Qualification Samples, and Test Data Package (3 copies) for SOHO Lot #2. The identification for these Qualification Samples is as follows:

Lot No.	Pkg. Serial No.	Tek Part No.
1453AN02-02	050	806-7735-55 (frontside)
1453CN11-03	078	806-7735-75 (backside)

Please give these samples and data to Dr. Ben Au and Dr. Russ Howard. If you have any further questions regarding these Deliverable Items, then please contact me immediately.

Regards,

Jon Ferrara

Jon Ferrara
NRL/SOHO Program Manager
Tek Microelectronics
CCD Products

Tektronix, Inc.
P.O. Box 500
Mail Stop 59-567
Beaverton, Oregon 97077
PHONE: 503-627-6865
FAX: 503-627-5560

copies: Dr. Morley Blouke, Dr. Ben Au, Dr. Russ Howard

Tektronix Inc
P.O. Box 500
Beaverton, Oregon 97077-0001
503 627-7111
503 627-5139 Fax

Tektronix
Test and Measurement

May 15, 1992

George Kowalski
Naval Research Laboratory
4555 Overlook Ave., SW
Bldg. 209, Room 138
Washington, D.C. 20375-5000

Attention: George Kowalski

Copies: Dr. Ben Au, Dr. Russ Howard, Dr. Morley Blouke

SUBJECT: SOHO LOT #3 QUALIFICATION SAMPLES & TEST DATA PACKAGE

Reference: NRL/SOHO Contract Number N00014-91-C-2052

We have successfully completed the Qualification Testing on the CCD samples from SOHO Lot #3. Please note thate Qualification Samples PASSED all of the required tests as follows:

1. Thermal Cycle (-55 to +125C, 25 cycles): No visual defects.

2. 100% Destructive Wire Bond Pull Strength.
   - Lot No. 1461AN05-04 (frontside CCD) had a mean and std. deviation of 10.6 grams, and 1.9 grams, respectively.
   - Lot No. 1461CN09-01 (backside CCD) had a mean and std. deviation of 11.0 grams, and 1.4 grams, respectively.

Note: Acceptable wire bond pull strength is greater than 2.5 grams.

3. Die Shear Strength Test.
   Both parts passed with greater than 10 kilograms die shear strength. (Acceptable is greater than 0.75 kilogram.)

Enclosed are the Qualification Samples, and Test Data Package (3 copies) for SOHO Lot #3. The identification for these Qualification Samples is as follows:

Lot No.	Pkg. Serial No.	Tek Part No.
1461AN05-04	074	806-7735-55 (frontside)
1461CN09-01	089	806-7735-75 (backside)

Please give these samples and data to Dr. Ben Au and Dr. Russ Howard. If you have any further questions regarding these Deliverable Items, then please contact me immediately.

Regards,

Jon Ferrara

Jon Ferrara
NRL/SOHO Program Manager
Tek Microelectronics
CCD Products

Tektronix, Inc.
P.O. Box 500
Mail Stop 59-567
Beaverton, Oregon 97077
PHONE: 503-627-6865
FAX: 503-627-5560

Tektronix
Test and Measurement

June 25, 1992

George Kowalski
Naval Research Laboratory
4555 Overlook Ave., SW
Bldg. 209, Room 138
Washington, D.C. 20375-5000

Attention: George Kowalski

Copies: Dr. Ben Au, Dr. Russ Howard, Dr. Morley Blouke

SUBJECT: SOHO LOT #4 QUALIFICATION SAMPLES & TEST DATA PACKAGE

Reference: NRL/SOHO Contract Number N00014-91-C-2052

We have successfully completed the Qualification Testing on the CCD samples from SOHO Lot #4. Please note that the Qualification Samples PASSED all of the required tests as follows:

1. Thermal Cycle (-55 to +125C, 25 cycles): No visual defects.

2. 100% Destructive Wire Bond Pull Strength.
   - Lot No. 1489AN03-03 (frontside CCD) had a mean and std. deviation of 11.7 grams, and 1.7 grams, respectively.
   - Lot No. 1489CN12-01 (backside CCD) had a mean and std. deviation of 10.2 grams, and 1.8 grams, respectively.

Note: Acceptable wire bond pull strength is greater than 2.5 grams.

3. Die Shear Strength Test.
   Both parts passed with greater than 10 kilograms die shear strength. (Acceptable is greater than 0.75 kilogram.)

Enclosed are the Qualification Samples, and Test Data Package (3 copies) for SOHO Lot #4. The identification for these Qualification Samples is as follows:

Lot No.	Pkg. Serial No.	Tek Part No.
1489AN03-03	101	806-7735-55 (frontside)
1489CN12-01	032	806-7735-75 (backside)

Please give these samples and data to Dr. Ben Au and Dr. Russ Howard. If you have any further questions regarding these Deliverable Items, then please contact me immediately.

Regards,

Jon Ferrara

Jon Ferrara
NRL/SOHO Program Manager
Tektronix
CCD Products

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Beaverton, Oregon 97077
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TECHNICAL PAPERS

Extreme UltraViolet Response of a Tektronix 1024x1024 CCD

D. Moses

Naval Research Lab, Code 4160.1
Washington, DC 20375-5000

J.-F. Hochedez

University Space Research Association
Washington, DC 22024

R.A. Howard and B. Au

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ABSTRACT

The goal of the detector development program for the Solar and Heliospheric Spacecraft (SOHO) EUV Imaging Telescope (EIT) is an Extreme UltraViolet (EUV) CCD (Charge Collecting Device) camera. The Naval Research Lab (NRL) SOHO CCD Group has developed a design for the EIT camera and is screening CCDs for flight application. Tektronix, Inc. have fabricated 1024x1024 CCDs for the EIT program. As a part of the CCD screening effort, the quantum efficiency (QE) of a prototype CCD has been measured in the NRL EUV laboratory over the wavelength range of 256 to 735 Angstroms. A simplified model has been applied to these QE measurements to illustrate the relevant physical processes that determine the performance of the detector.

2. INTRODUCTION: THE EIT MISSION

SOHO is a joint European Space Agency (ESA) and NASA project within the Solar Terrestrial Science Scientific Program. The overall objective of SOHO is the study of the solar interior and atmosphere. The solar atmosphere is defined in this context to extend from the solar photosphere out through the solar wind. The orbital station of the SOHO spacecraft is the inner Lagrangian point (~0.99AU). This location allows the acquisition of *in situ* measurements of the solar wind to compare to the remote measurements of the inner solar atmosphere and solar wind. The combined simultaneous study of all levels of the Sun and

the Sun's interaction with interplanetary space will provide a new perspective on solar-terrestrial physics.

The contribution of the EIT to the SOHO project is the provision of images of the full solar disk in four EUV passbands. The passbands are determined by the combination of thin aluminum visible light rejection filters and multilayer mirrors tuned to optimally reflect the desired passband. These EUV passbands have been chosen so that the image from each passband is dominated by emission lines formed at a temperature characteristic of a different level of the solar atmosphere. The solar structures observed in the EIT passbands range from the chromospheric network to hot coronal loops (corresponding to temperatures ranging from 6×10^4 K to 3×10^6 K). The scientific performance of the EIT is summarized in Table 1. The primary scientific questions addressed by observations of these solar structures are the still-open problems of the heating of the solar corona and the acceleration of the solar wind. The EIT observations will provide supporting information for many other scientific programs conducted by the SOHO effort including near real-time pointing information for the nonimaging SOHO instruments.

In order to achieve the scientific goal of determining the plasma properties of structures in the solar atmosphere, the EIT must make high precision measurements of emission through each of the four passbands. A thinned back-illuminated CCD was the only detector system available at the inception of the EIT project that fulfilled the dual EUV solar imaging requirements of high photometric accuracy and appropriate exposure times. The optical system of EIT is arranged so that the images through the four passbands are confocal. The specific passband for any chosen image in an EIT observing program is selected by an aperture mask that blocks the optical paths of the other three unwanted passbands. Thus, only one detector is needed; lowering weight and power requirements, as well as mostly removing detector degradation as an explanation of the relative changes in efficiencies of each of the four passbands.

Table 1

EIT Scientific Performance
Image Bandpass Properties

Wavelength Peak (Angstroms)	Dominant Emission Line	Characteristic Emission Line Ion Temperature (Kelvin)
304	He I	6×10^4
284	Fe XV	3×10^6
195	Fe XII	1.6×10^6
171	Fe IX	1×10^6

3. THE EIT CCD CAMERA

The EIT CCD camera has been developed to use a custom fabricated Tektronix 1024 x 1024 CCD. The design of the SOHO CCDs are based on the commercial Tektronix TK1024 backside illuminated CCD imager. Significant modifications were made in the areas of mask design, MPP implant, low-noise on-chip output amplifier, backside treatment, and packaging. These modifications were an extension of a

design initiated by the NASA/GSFC Space Telescope Imaging Spectrometer (STIS) program.

Details of the camera design, the CCD chip level evaluator system, and the visible light test results are given in these Proceedings by Howard[1]. The properties of the EIT CCD are summarized in Table 2.

Table 2
Properties of the EIT CCD

Format:	1024 x 1024 pixels
Gate Structure:	3-phase with MPP implant barrier in phase 3
Pixel Size:	21 microns x 21 microns (approximately 3 x 3 arcsec^2 in the focal plane)
Readout Rate:	50 kpixels/sec
Full Well	≥150,000 electrons
Dark Current:	≤10 e/pixel/sec at -80 °C
Readout Noise:	≤10 e/pixel at -80 °C

Unique to the back-illuminated Tektronix CCD is the necessity to extend the parallel transfer time to greater than 200 microseconds in order to obtain adequate full well depth. We speculate that this difference between the front-side and back-side illuminated devices comes from additional impedance incurred in the transfer of clock signals from the bond wire of the package to the polysilicon gate structure of the device. Since the back-illuminated devices are constructed with the gate structure side of the device bonded an inert supporting substrate, electrical access to the gate structure is more complicated than with the front-illuminated devices. Fortunately, the serial transfer structure is not particularly sensitive to this effect. The optimal serial transfer clock rate is the same for the back-illuminated and front-illuminated devices. Thus, the total time for readout of the back-illuminated CCD is still approximately 22 seconds,which is well within the mission requirement.

4.NRL EUV FACILITY

The NRL EUV calibration facility consists of an EUV monochromator, an EUV light source, NIST calibrated reference photodiodes, and an accommodation of both the CCD 'chip evaluator' system referred to above, as well as, the flight design EIT 'brassboard' camera unit. Extensive efforts were made to maintain an ultra-clean vacuum environment in the EUV facility, in order to avoid contamination of the CCD. Since the CCD was operated at cryogenic temperatures, it was expected that any potential contaminant present in the vacuum would condense on the surface of the CCD and act as an EUV filter. Three vacuum turbopumps are used to differentially pump the monochromator without risk of hydrocarbon contamination of the vacuum from backstreaming in the pump. The consistency of EUV quantum efficiency measurements obtained with this system demonstrates the success with which these instrumentation goals were achieved.

The monochromator is a grazing incidence design by Salle and Vodar[2]. This design fixes the entrance slit to be at the same distance from and at the same

angle to the grating. A simple, linear translation mechanism can be constructed which allows the entrance slit and grating to be moved, with the above constraint, so that the Rowland circle pivots about the exit slit as the monochromator scans wavelength. This design provides a fixed exit slit and a fixed orientation of the exit beam. This last property of the monochromator design is particularly useful in allowing the location of the CCD 'chip evaluator' (with its associated, bulky electronics rack) to be fixed in space. Since no further optics are required to direct the EUV light onto the CCD, the monochromator provides the greatest throughput for a given source.

Glow discharge radiation sources utilizing EUV emission lines of noble gases are used to illuminate the monochromator. A capillary discharge tube of the type developed by Hunter as well as a magnetic confinement source of the type developed by Damany are used in the NRL facility. Both sources are operated in a windowless configuration to obtain maximum throughput. This configuration requires rapid differential pumping to maintain a pressure of 10^{-5} torr in the monochromator while allowing pressures of up to 10^{-1} torr in the light source. The properties of the monochromator and light sources are summarized in Table 3.

Table 3

NRL EUV Monochromator System Characteristics

Design:		Romand-Vodar
Wavelength Range:		110 to 1450 Angstroms
Grating Ruling:		400 lines per mm replication
Grating Surface:		Gold
Grating Radius:		2998.3 mm
Grazing Angle of Incidence:		82°
Entrance Slit to Grating Spacing:		418 mm
NIST Calibrated Reference Detectors:		Windowless Alumina Photodiode
		XUV-100C Silicon Photodiode
Primary Emission Lines:	Ion	Wavelength (Angstroms)
	He II	256
	He II	304
	Ne II	461
	He I	584
	Ne I	735

5.CCD EVALUATION

The state of the art of EUV CCD evaluation is discussed in detail by Hochedez[3]. For the purpose of this work, we consider only the average response of the CCD over the region of the device which is illuminated by the diverging exit beam of the monochromator. This beam is limited by an aperture plate located at the entrance of the CCD test chamber. This aperture serves the dual purpose of defining the EUV illumination to a region within the active area of the reference diodes and providing a last contamination barrier between the

monochromator and the CCD test chamber. Because of the different mechanical and vacuum accommodations for the 'chip evaluator' camera and the flight design 'brassboard' camera, the projection of the divergent EUV beam on the CCD is different for the two cameras. The beam size at the CCD in the 'chip evaluator' configuration is approximately 6.3mm in diameter while the beam size in the 'brassboard' configuration is approximately 9.4mm in diameter.

The procedure for a measurement is as follows:

1)A reference diode is inserted into the beam to measure the net flux.
2)The reference diode is removed from the beam and a computer controlled shutter exposes the CCD to the beam.
3)The CCD image is read into memory.
4)A glass window is inserted into the beam and a second CCD exposure is made and read out to determine the combination of visible light and other background signal in the CCD.
5)The reference diode is re-inserted into the beam to check for drift.

EUV QE measurements of the CCD designated to be used in the EIT 'brassboard' camera were being made with the 'chip evaluator' camera during the time that experimentation with the clocking pattern and voltages was being conducted. As described elsewhere (Howard, op. cit.), extensive changes were made in the way the CCDs were operated in order to optimize performance. Thus comparison of QE measurements during this time is linked to the detailed experimentation with CCD operation. Furthermore, the CCD exhibits significant nonuniformity in response from pixel to pixel, so that the average QE which was measured at any time depended on the specific orientation of the CCD EUV illumination. Throughout all of the EUV QE measurements with all of the various operating modes of the CCD, a variation on the order of a factor of two was seen in the short wavelength QE measurements while a variation on the order of a factor of ten was seen in the long wavelength QE measurements. Although interesting detector physics may be explored by a detailed study of these variations in QE with non-optimal CCD operational modes, this investigation is limited to a determination of the detector properties that would be encountered by the EIT instrument in the flight configuration. The QE measurements for a given operating configuration were stable to within the accuracy of the reference diode measurement of the incident UV radiation (~10%). Thus, this paper is restricted to the discussion of the QE measurements made with the flight design 'brassboard' camera unit, which utilizes the optimal operating mode for this CCD (as established by the 'chip evaluator').

The QE measurements in this paper will be expressed in terms of detective quantum efficiency: The QE is the ratio of the charge detected by the device to the total charge that should have been deposited in the device, if all the incident EUV radiation were converted into detectable charge. At EUV photon energies, we assume that one electron-hole pair is generated for every 3.65eV of incident radiation energy. The total photon energy incident upon the CCD is the product of the intensity of the EUV beam as determined by the calibrated diode, the energy per EUV photon of the wavelength selected by the monochromator, and the EUV exposure time for the CCD determined by the computer controlled shutter. The error in the QE measurements is dominated by the uncertainty in the measurement of the incident EUV beam. This error is on the order of 10% for all of the measurements, so it is not listed separately for each QE. The average QE over the central region of the 'brassboard' CCD, as measured at the NRL EUV

facility with the flight configuration EIT brassboard camera, is listed in Table 4.

Table 4
Detective Quantum Efficiency of the Tektronix 1024x1024 CCD

Wavelength (Angstrom)	Quantum Efficiency
256	28%
304	24%
461	21%
584	9%
736	4%

Variations in the QE over the CCD pixel field is obvious on some scales from the images of the EUV beam. The image of the EUV beam at 304 Angstrom is presented in Figure 1, and the image of the 736 Angstrom beam is presented in Figure 2. The divergent EUV beam varies gradually over the illuminated region of the CCD. The small scale structure of the images in Figures 1 and 2 corresponds to pixel to pixel variations in EUV response. Although there are a few dust particles on the CCD, most of the small scale features are intrinsic to the device, presumably byproducts of the back-side etch process.

Variations in the EUV response are also present on spatial scales of 200-400 pixels. These variations are stronger in the longer wavelength images. The localized brightening in the upper quarter of the EUV image in Figure 2 is a clear example of part of one of these regions of enhanced EUV response. These regions are clearly mapped in the dark current image presented in Figure 3 as regions of reduced dark current. A close visual inspection of the back-side surface of the CCD reveals that these regions of increased QE and reduced dark current are regions where the backside etch was slower than over most of the CCD. The most descriptive term (informally used in the NRL CCD group) for these regions is 'hills' on the back-side of the device. The majority of the back-side surface is in the 'valley' region. As can be seen in Figure 3, the central area of the CCD, over which the NRL EUV facility was configured to measure average QE, mostly consists of the more deeply etched 'valley' region.

We expect, from the techniques used to fabricate these devices, that the 'hill' regions will have a higher concentration of the back-side implanted p^+ material. The p^+ dopant is implanted in the back-side of the CCD after the thinning etch in order to overcome the surface potential generated by the back-side oxide interface states. Since this implant most strongly influences charge deposited near the back-side surface of the device, the effect of implant concentration will be greater for those wavelengths which have a shallow penetration depth in silicon. In the wavelength regime explored by these EUV measurements, the penetration depth decreases with increasing wavelength. Thus, the QE variation associated with the 'hill' structures is greater for the longer wavelength image of Figure 2 than for the shorter wavelength image of Figure 1. The variations of dark current with the 'hill' structures indicate that, at the cryogenic temperatures at which the devices are operated, the dominant source of dark current is the surface states.

The variation in etch depth of the back-side thinning process is difficult to precisely control in a production environment. Preliminary observations of the

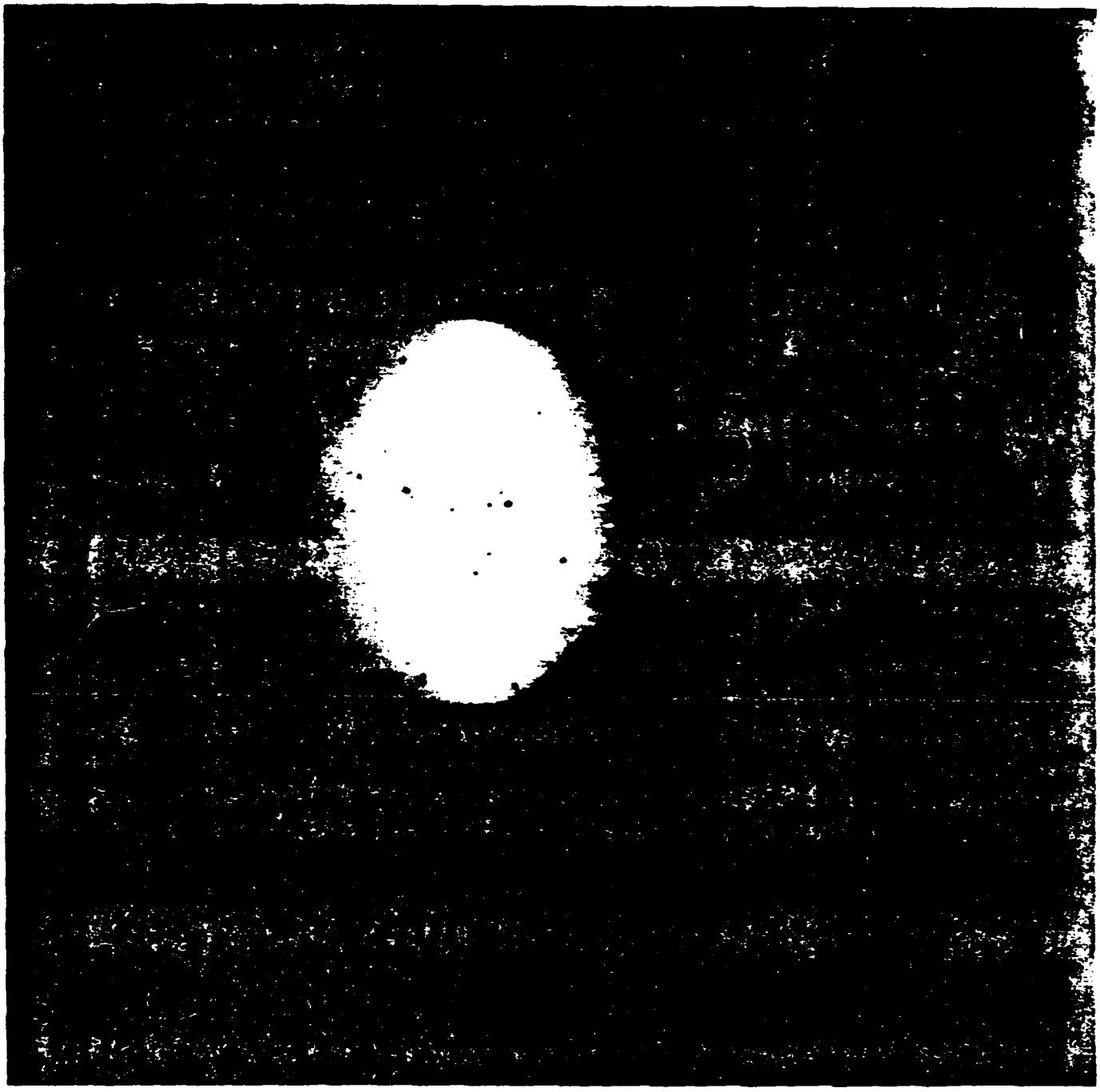

Figure 1.
CCD Image of 304 Angstrom Beam (NRL EUV Facility)

Figure 2.
CCD Image of 736 Angstrom Beam

Figure3.
CCD Dark Current Image (-68°C Device Temperature)

'flight candidate' CCD lots indicate that a more even etch was obtained in the fabrication of these devices than in the earlier 'brassboard' devices. Further testing is required to verify these early indications.

Although the variations in QE observed in the 'brassboard' CCD are significant, even the 'brassboard' device could be used to achieve the scientific objectives of the EIT mission. The 'brassboard' images in Figures 1, 2, and 3 have been contrast-enhanced so that the effects discussed are exaggerated to be easily visible in the Proceedings reproduction. A flat-fielding image processing procedure could take out all of the QE variations in the 'brassboard' camera CCD with an acceptable level of scientific data degradation. However, the desire for maximum scientific return from this rare orbital observation opportunity, combined with the daunting computational difficulties associated with the wavelength dependence of the required flat-fielding, leads us to strive to obtain the most uniform response possible in the 'flight candidate' CCDs.

6. EUV RESPONSE MODEL

In order to better understand the EUV performance of the EIT CCD camera, as well as the performance of the total EIT instrument, it is useful to attempt to apply a simple physical model to the QE observations. Since the use of a glow discharge source allows QE measurements in this regime of the EUV only at the specific wavelengths that bright emission lines are available, it is important to anticipate the EUV performance of the CCD at the continuum of wavelengths that the EIT telescope will transmit to the detector. The technique of using the multilayer reflectivity of the EIT telescope optics to define the wavelength bandpass of the four channels requires that the 'off-band' contributions to the total signal in any channel be well understood before solar plasma diagnostics can be derived from the observations.

A useful model of the performance of back-illuminated CCDs has been presented by Blouke, Delamere and Womack (1991)[4]. This model divides the CCD into four regions, discussed here in the order that the incoming radiation interacts with the device. The first region is the back-side native oxide which forms on the surface of the CCD. Incoming light is either reflected, absorbed, or transmitted through this region (as is calculated with well known optical constants, e.g. Palik[5]) without otherwise contributing to the signal collected by the CCD. The second region is the p^+ back-side implant region which is designed to overcome the potential well created by trapped charge in the native oxide and to accelerate toward the CCD accumulation wells the electrons generated by the photons absorbed in this shallow region. Charge generated by absorption of photons in this second region diffuses out of the region under the influence of the electric field created by the p^+ implant. The third region is a field-free region which is bounded on one side by the p^+ implant region and on the other side by the depletion region of the CCD accumulation well. Charge generated by photon absorption in this third region, or transported into this region from the p^+ back-side implant region, diffuses through the third region, influenced only by the gradient of the charge distribution. The fourth region is the depletion region of the CCD accumulation well. All charge generated in the depletion region as well as all charge transported into this region from the field-free region is collected as signal for eventual readout. Any charge

losses after accumulation in the depletion region are described by charge transfer efficiency (CTE) effects which are not included in this model.

The efficiency of collection of charge generated by absorption of incident EUV radiation is determined by solving a steady-state continuity equation for the mobile electronic charge within each region. In every region, the absorption of the incident photon beam that is transmitted through the previously encountered regions is a source of charge. In the first region, which is electrically insulating, no photo-generated charge is transferred out of the region. The second region is characterized by a back surface recombination velocity (charge lost through interaction with the oxide interface), and an electric field which, for computational simplicity, is assumed to be constant throughout the region. Both the second and third regions are characterized by the electron recombination rate, electron mobility, and electron diffusion constant of the bulk material. The fourth region is the CCD accumulation well, for which only the current from the field free region interface and the photo-generated charge within that region are of interest. Thus, the application of the model involves the solution of the continuity equation in the second and third regions, subject to the boundary conditions of each region, to obtain the current into the accumulation well.

This model has been applied to the QE measurements discussed in Section 5. The parameters of the best fit of the model to the data are listed in Table 5. The QE predicted by the best fit model is plotted in Figure 4 against the QE observations from Section 5.

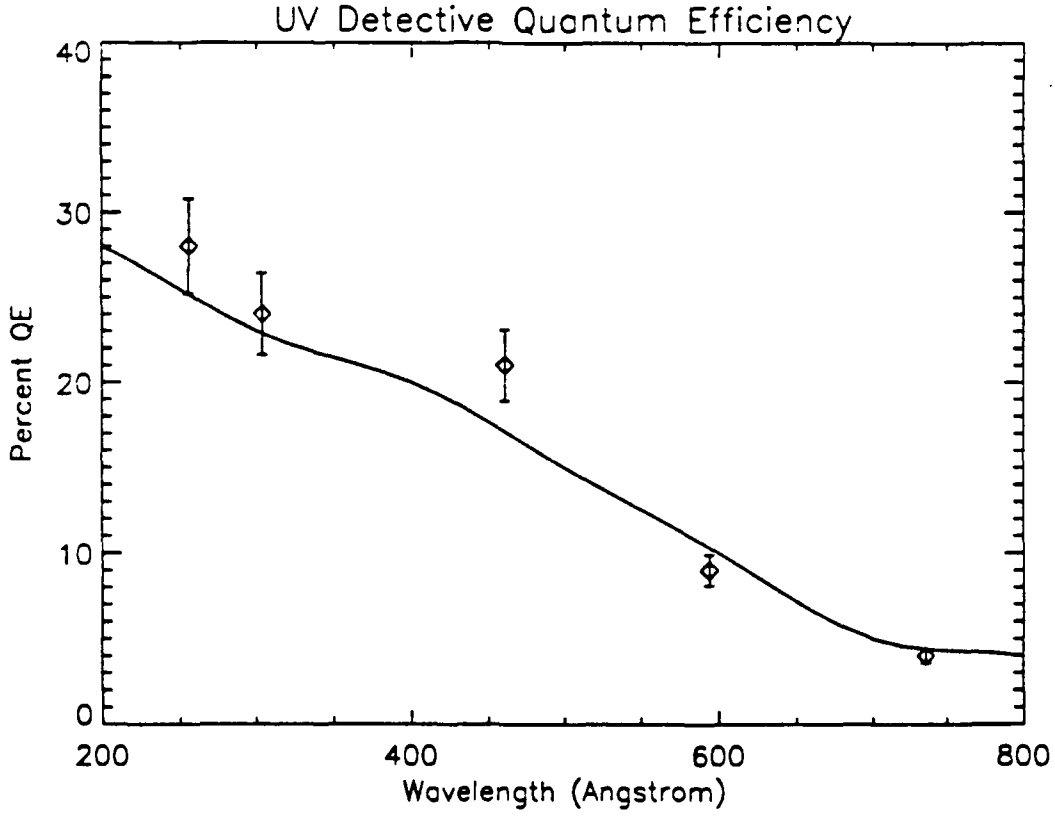

Figure 4. Measured QE and Best Fit QE Model

Table 5
Parameters Of the Best Fit CCD QE Model

Total Depth of CCD	15.0 microns
Depth of Depletion Region	8.0 microns
Depth of p^+ Back-side Implant Region	0.1 microns
Native Oxide Depth	$13 \cdot 10^{-3}$ microns (130 Angstroms)
Back-side Surface Recombination Velocity	$4 \cdot 10^5$ cm/sec
Back-side Implant Region Electric Field	$-5 \cdot 10^3$ V/cm
Electron Recombination Lifetime	40 microseconds
Electron Diffusion Constant	25 cm^2/sec

7. EIT CALIBRATION PROGRAM

The EUV evaluation work described in this paper is only the first step in the calibration program for the EIT instrument. Following device screening at NRL, a more extensive calibration of the CCD will be conducted at the Lockheed Palo Alto Research Laboratories (LPARL). The calibration effort at LPARL will include QE measurements at wavelengths shorter than those described above (114 Angstroms and 171 Angstroms), as well as more comprehensive explorations of the departure from flat-field EUV response. The LPARL facility was used successfully to calibrate the CCD that is now returning excellent images from the Soft X-Ray Telescope on the Yohkoh spacecraft. Agreement between the NRL and LPARL measurements of QE will provide an extra level of confidence for a photometric calibration in what has historically been a difficult region of the spectrum. Following the LPARL calibration of the CCD camera, a calibration of the fully integrated EIT instrument will be conducted by the Institut d'Astrophysique Spatiale at the synchrotron beam facility at Orsay, France. The entire screening and calibration procedure will be carried out on a flight design 'brassboard' unit prior to the calibration of the flight hardware to evaluate improvements in the procedure.

8. ACKNOWLEDGEMENTS

The support of Glenn Holland of the Naval Research Laboratory was essential in all aspects of the refurbishment of the NRL EUV facility. The laboratory support of David Roberts, Robert Chaimson, and Charles MacDonald is also gratefully acknowledged. Helpful suggestions were made by Drs. C. Brown, G.E. Brueckner, R. Catura, J. Lemen and D. Michels. The design and fabrication of the EIT camera systems is being carried out by Analytx Electronic Systems in Hudson, NH. This work is funded by the NASA International Solar Terrestrial Physics Program and the Office of Naval Research.

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Charge Transfer Efficiency Measurements at Low Signal Levels on STIS/SOHO TK1024 CCD's

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ABSTRACT

The charge transfer efficiency (CTE) characteristics of the Tektronix 1024 × 1024 CCD being developed for STIS/SOHO space imaging applications have been characterized at different signal levels, operating conditions, and temperatures using a variety of test methods. A number of CCD's have been manufactured using processing techniques developed to improve CTE, and test results on these devices will be used in determining the final chip design. In this paper, we discuss the CTE test methods used and present the results and conclusions of these tests.

1. INTRODUCTION

The charge coupled devices (CCD) being developed for the Space Telescope Imaging Spectrograph (STIS) and Solar Heliospheric Observatory (SOHO) space instruments will be based on the test devices currently being fabricated by Tektronix, Inc.[1][2]. These 3-phase, four-quadrant readout devices contain 1024× 1024, 21 μm^2 pixels with 20 overclocked pixels on both ends of the two serial registers. Charge can be read out through any or all of the four amplifiers. Figure 1 is a functional diagram of this CCD showing the charge movement in the four-quadrant readout mode and the amplifier names. During this development phase, a number of devices have been fabricated with variations in the wafer manufacturing process, with the goal of producing a CCD that meets the program design requirements. The performance improvements made possible by multi-pinned-phase (MPP) implants have been well documented, so all current test devices are of this type.

Important performance requirements, especially for the STIS application, are very low dark current, low readout noise, and high charge transfer efficiency (CTE) at low signal levels as might be encountered with faint star images on a black background. In this paper, we discuss a few different methods of measuring CTE, the correlation between the methods, and the results of tests on a few different CCD's.

2. CHARGE TRANSFER EFFICIENCY MODELING

The charge transfer efficiency is a measure of the fraction of a charge packet that is transferred from one pixel to the next as it moves through the array. Some CTE measurements are quoted on per transfer basis, however, this becomes confusing when comparing devices with different numbers of phases per pixel, so we will define CTE on a per pixel basis. Charge transfer efficiency is signal dependent with large charge packets yielding higher values. CTE can be measured for both the parallel and serial directions, however, it is the parallel CTE that usually limits the ultimate performance of the CCD. Charge transfer efficiency can be modeled by a simple exponential expression of the form:

$$S_r = S_i C^n \tag{1}$$

where

S_r = signal after n transfers (electrons)
S_i = initial signal (electrons)
C = charge transfer efficiency (CTE)
n = number of transfers

Figure 2 shows a plot of percent of initial charge remaining as a function of number of transfers for different values of CTE between 0.99800 and 0.99999 [3]. Most of the CTE measurements we have made fit this curve very well, however, these curves assume constant CTE as the signal level changes. For large values of CTE (>0.99990) or small numbers of transfers, the curve can be approximated by a straight line.

3. CHARGE TRANSFER EFFICIENCY TEST METHODS

Measurements of CTE on the 1024 × 1024 device have been verified primarily using three different methods. These methods are Fe^{55} x-ray response, the Extended Pixel Edge Response (EPER) and Charge Injection through one of the output amplifier(s).

The Fe^{55} x-ray response method [4] is based on the response of a CCD to x-ray photons from the radioactive source Iron-55. Each photon that is absorbed by the silicon produces an average of 1620 electrons. Where the photons are absorbed within the frontside depletion region and not too close to the boundary between two pixels, all of the electrons will be collected within one pixel and are called single pixel events. Only a small fraction of the total number of interactions produce single pixel events.

To measure parallel CTE using the Fe^{55} x-ray response method, the CCD is exposed to a flat field of x-ray photons. The device is then read out and a scatter plot made, showing signal as a function of vertical position (row) within the CCD for each event. Figure 7 shows a plot of parallel CTE at -80 °C. The CTE can be calculated by measuring the final signal level after n transfers using the following expression:

$$C = \left(\frac{S_r}{S_i}\right)^{\frac{1}{n}} \tag{2}$$

where

S_r = signal after n transfers (electrons)
S_i = initial signal (1620 electrons)
C = charge transfer efficiency (CTE)
n = number of transfers

The Extended Pixel Edge Response method measures the charge lost to successive pixels by a known intial signal as it is shifted through the array. Typically, the CCD is exposed to a flat field of light to produce a charge amplitude where we want to measure the CTE. The shutter is then closed and the device is read out, depleting the charge in the array behind the image. Theoretically, there should be a perfect transition from full charge to no charge at the trailing edge of the image if there were no transfer loss. With non-perfect CTE, some charge is lost from the flat field to the trailing pixels and is called deferred charge. By overclocking the array and measuring the amount of deferred charge, the CTE can be calculated:

$$C = \left(\frac{S_i - S_d}{S_i}\right)^{\frac{1}{n}} \tag{3}$$

where

S_d = deferred charge in trailing pixels
S_i = initial signal (flat field level)
C = charge transfer efficiency (CTE)
n = number of transfers

A third method of measuring CTE uses charge injection through the output amplifier reset transistor and essentially operates the CCD in reverse. Figure 3 shows a schematic of one of the output amplifiers and the end of the serial register. The reset transistor gate, RGx, is connected to the reset drain, ODx, biasing the transistor on so the drain voltage appears at the output node. Charge is injected by using the last gate, LGx, as a sample gate to allow charge to flow from the output node to the summing well, SWx. By setting the reset transistor drain voltage to different voltages below the channel potential, the amount of injected charge can be adjusted. On these devices this voltage was set typically between 13 and 15 volts.

Serial CTE can be measured by gating charge into one end of the serial register for every 25th pixel or so and then read out at the opposite end of the register. The amount of deferred charge can be measured in the pixels trailing the injected charge packet and the CTE can be calculated from the EPER equation. Figure 4 shows the C output with approximately 1600 electrons injected for every 25th pixel into the D end of the serial register.

To measure parallel CTE, two different methods of charge injection can be used. The first method injects charge into one serial register and is read out through the other serial register. For example, assume charge is injected into the A amplifier and read out through the C amplifier. First, the A/B serial register is filled with charge of a known level. This charge is then shifted from the serial register, through the transfer gate and into the parallel section of the CCD. A number of parallel transfers are then made without injection from the serial register. The serial register is filled with charge again and the process is repeated until the array is filled with charge in every 25th line. The array is then read out normally through the C amplifier. Figure 5 shows the rows of injected charge followed by the deferred charge as each line was clocked 1024 times down through the array. The CTE is calculated by measuring the deferred charge and using the EPER equation.

In the second method, charge is injected into the same serial register as is used to read out the device. This method can be used for devices with only one serial register or one output amplifier. For our tests, we injected charge into the D amplifier and read out through the C amplifier. The C/D serial register is first filled with charge, and then it is shifted up into the parallel section of the array. A number of shifts are made before another line of charge is again shifted up into the array. This process is repeated until the array is filled with charge in every 25th line after which it is read out normally through the C amplifier. The first line read out has been shifted twice, once up and once down, whereas the last line has been shifted 1024 lines up and 1024 lines down.

A rough transfer efficiency can be calculated using the same techniques as is used for the Fe^{55} x-ray response test method, however, the number of transfers is now twice the number of rows since the charge was shifted both directions. This calculation is a reasonable approximation of the actual CTE if the assumption is made that the CTE is good and that it is constant for all signal levels. If this were the case, the injected signal should have deferred charge tails of approximately equal sizes extending on both sides of the base. Figure 6 shows a magnified portion at the base of the injected pulse after readout. Note that the deferred charge tail on the right side, corresponding to the shift down, contains approximately five times the amount of charge than the tail on the left side.

In reality, the CTE is usually much worse for small signals so that the small amount of deferred charge during the shift up will be "swept" up as the signal is shifted back down through the array. In the limit, the actual CTE will approach what would be calculated using half the total number of transfers.

Another factor that could influence the symmetry of the deferred charge tails is that the parallel CTE is different in one direction than in the other. Although this is unlikely in the design of the CCD, the speed of clocking in each direction could have a large effect on the apparent CTE [5] due to a characteristic known as charge transfer hysteresis (CTH). In our tests, the shift up was completed in about 1/25 of the time that the shift down/readout took place.

The actual CTE will then fall somewhere between what is calculated for the total number of transfers and what is calculated for half that number. For the devices we have tested and the method used, we find that the CTE more closely approximates that measured by other methods, when calculated using only the number of downward transfers.

4. TEST RESULTS

Charge transfer efficiency measurements were performed on a number of devices with known different CTE's to compare the different methods. Figure 7 shows the Fe^{55} response and the CTE calculation for one of the devices. Figure 5 shows the results of the CTE calculation for charge injection at 1600 electrons through the A amplifier and readout through the C amplifier, using the EPER equation. Finally, Figure 8 shows a 1600 electron charge injected through the D amplifier and read out through the C amplifier. In this case, the CTE is calculated using the Fe^{55} equation with half the total number of transfers. All three methods yield CTE numbers which are in good agreement.

Tests were performed on this device at some lower signal levels using charge injection through the D amplifier. Figure 9 shows the response and CTE calculations at 400, 150, 50, and 10 electrons. As expected, the CTE decreases at these lower charge levels.

Figures 10 shows Fe^{55} x-ray plots for three vertical areas on a device that was irradiated with 2 Krads of protons. This test was performed to determine the effectiveness of different thicknesses of shielding and plots of the areas with lead brick, 4 mm tantalum, and no shielding are shown [6]. Note how the x-ray line diverges for higher numbered rows.

Figure 11 shows the plots using charge injection at every 25th row for the same signal level as Fe^{55} x-rays. The CTE calculated using this method with half the number of shifts, yields a number which is very close to the Fe^{55}

x-ray method. Note the increasing deferred charge tail as the signal level decreases. The amount of charge in the deferred tail is equal to the amount of charge lost from injected signal.

Figure 12 shows the Fe^{55} response and a 1600 electron charge injection through the D amplifier, for another device that received a 2 Krad proton dose. In this device, the lower half of the device was unshielded and the upper half was shielded with a lead brick. All charge in the shielded region had to be shifted through the unshielded region to reach the serial register.

6. CONCLUSIONS

As charge coupled device arrays become larger with reduced amplifier read noise and greater dynamic range, and the subsequent use of these devices at lower signal levels, the need for good CTE at low signal levels will become an even greater requirement. The x-ray response method can be used with a variety of radioactive sources to allow CTE measurements between 30 and 6000 electrons although this requires a different source for each level [7]. The EPER method can theoretically be used at any signal level for measuring both serial and parallel CTE.

The principal advantages to the charge injection method are a totally electronic measurement system, with no flat field light or x-ray source necessary. This could be advantageous on a long duration space mission to measure CTE degradation due to the space radiation environment and in other remote applications where it is impractical to have an external source of pixel stimulation. This method also offers flexibility charge level and can be used for both parallel and serial CTE measurements. Finally, the results obtained by this method have been shown to be consistent with the other two proven methods.

6. ACKNOWLEDGEMENTS

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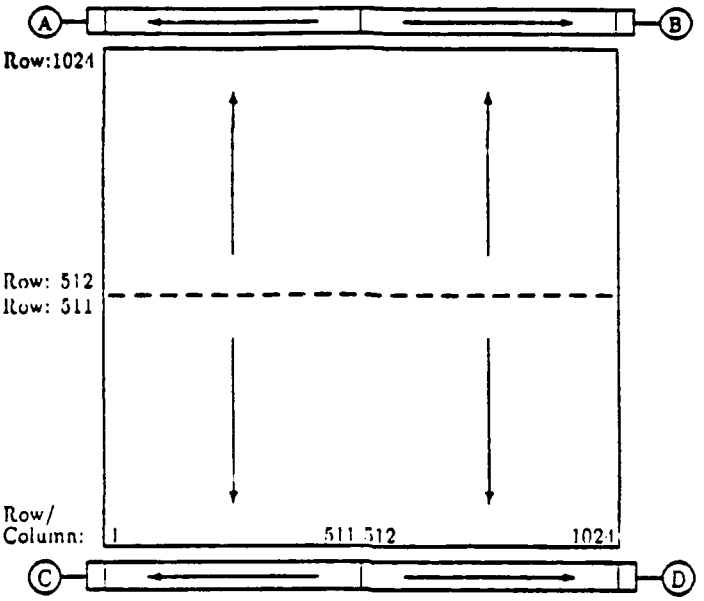


Figure 1: TK1024 functional diagram showing 4-quadrant readout mode

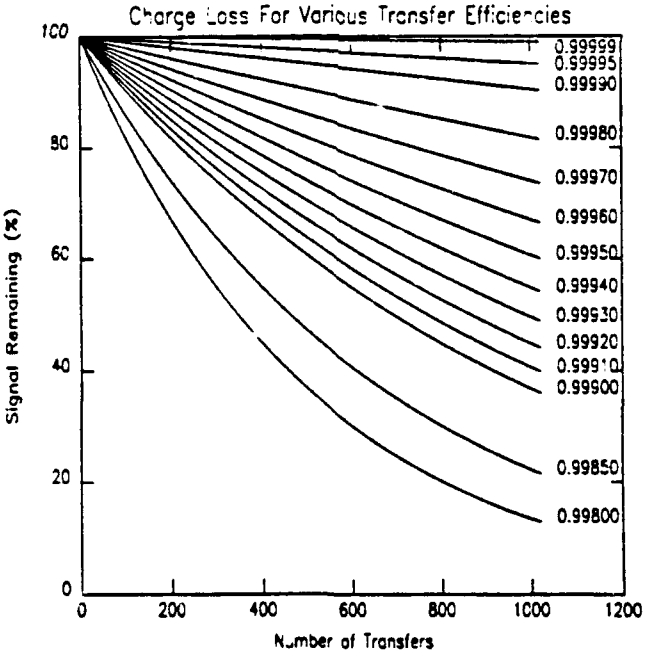


Figure 2: Theoretical charge loss for different values of CTE

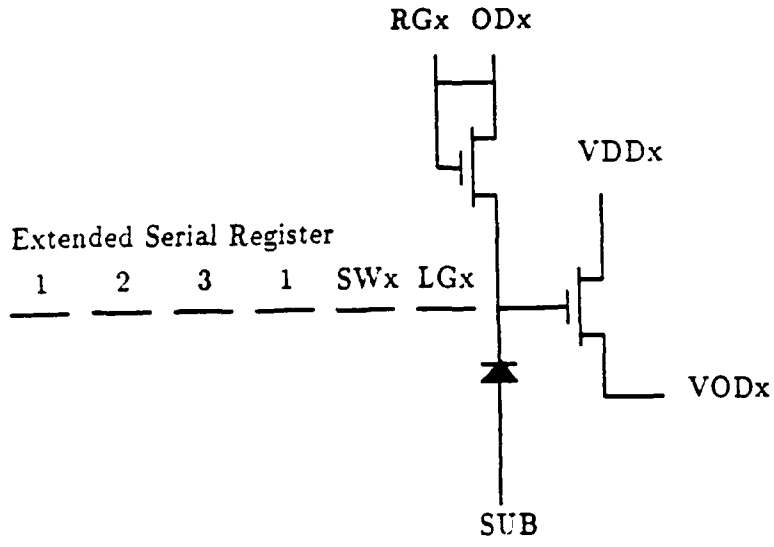


Figure 3: Schematic of the output amplifier configured for charge injection.

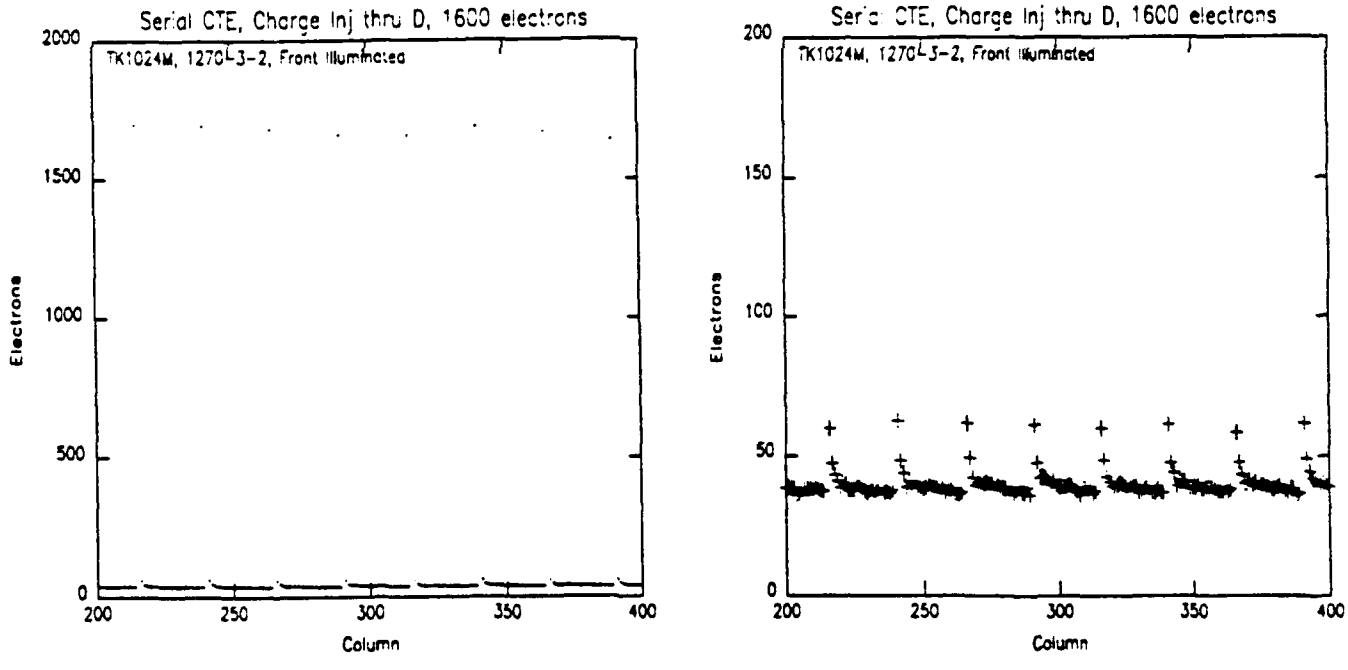


Figure 4: Serial CTE at 1650 electrons with charge injection through D and readout through C, expanded to show deferred charge, CTE = $\left(\frac{1650-38}{1650}\right)^{\frac{1}{1024}} = 0.999977$

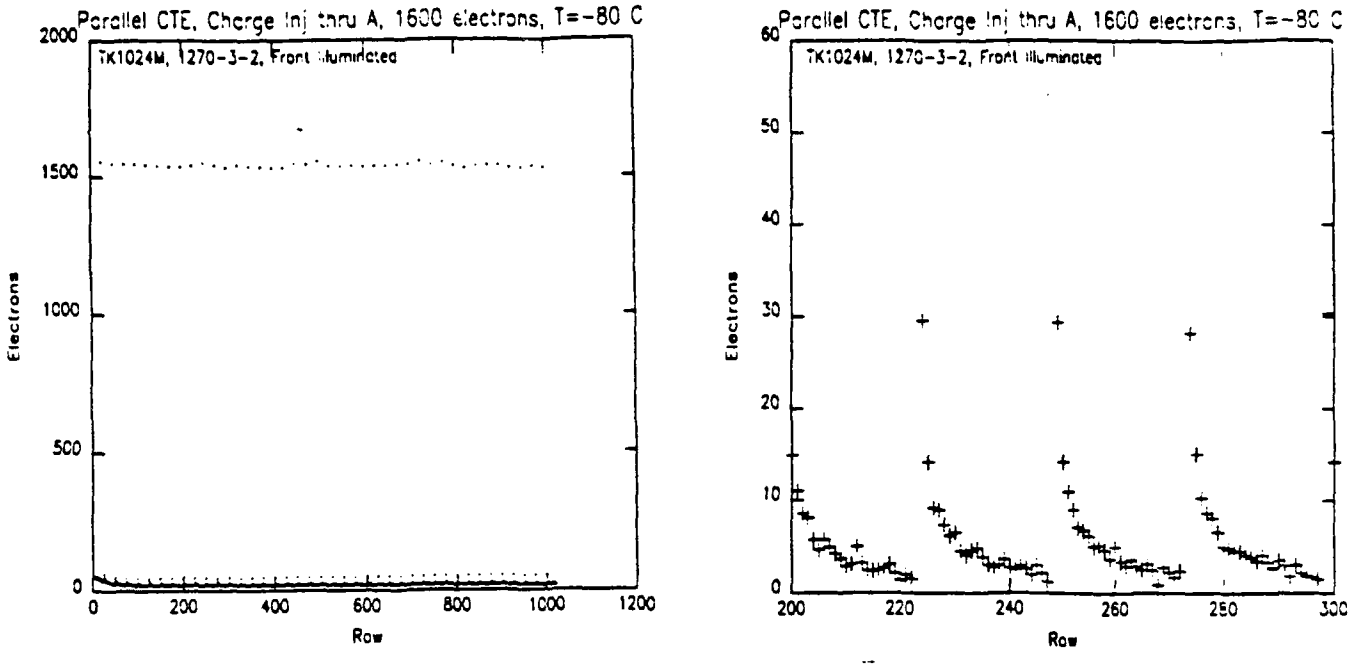


Figure 5: Charge injection through the A amplifier with readout through C with magnified section showing deferred charge, CTE = $\left(\frac{1620-70}{1620}\right)^{\frac{1}{1024}} = 0.999957$

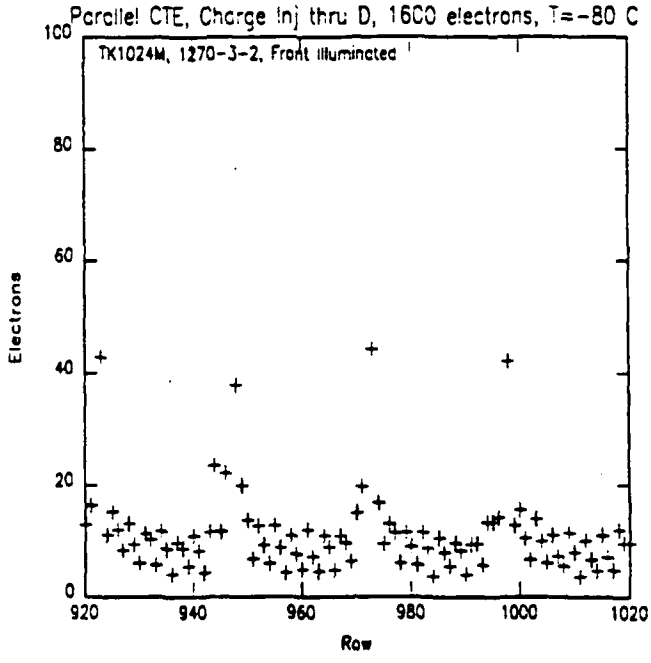


Figure 6: Charge injection through D amplifier with readout through C, magnified to show deferred charge tails

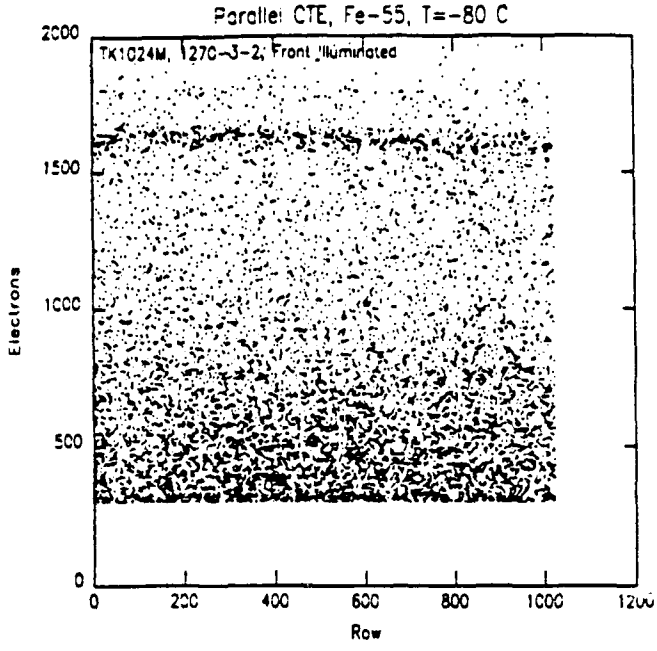


Figure 7: Fe^{55} x-ray response, CTE = $\left(\frac{1620-67}{1620}\right)^{\frac{1}{1024}}$ = 0.999959

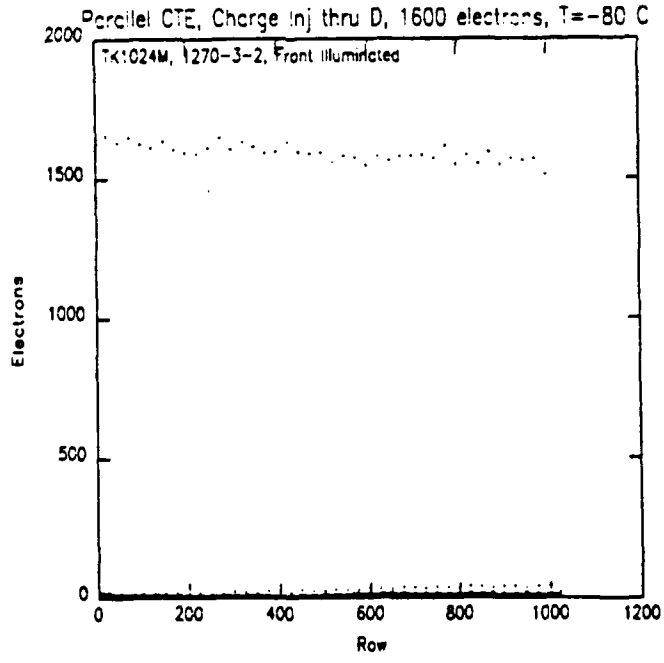


Figure 8: Charge injection through D amplifier with readout through C, CTE = $\left(\frac{1620-70}{1620}\right)^{\frac{1}{1024}}$ = 0.999957

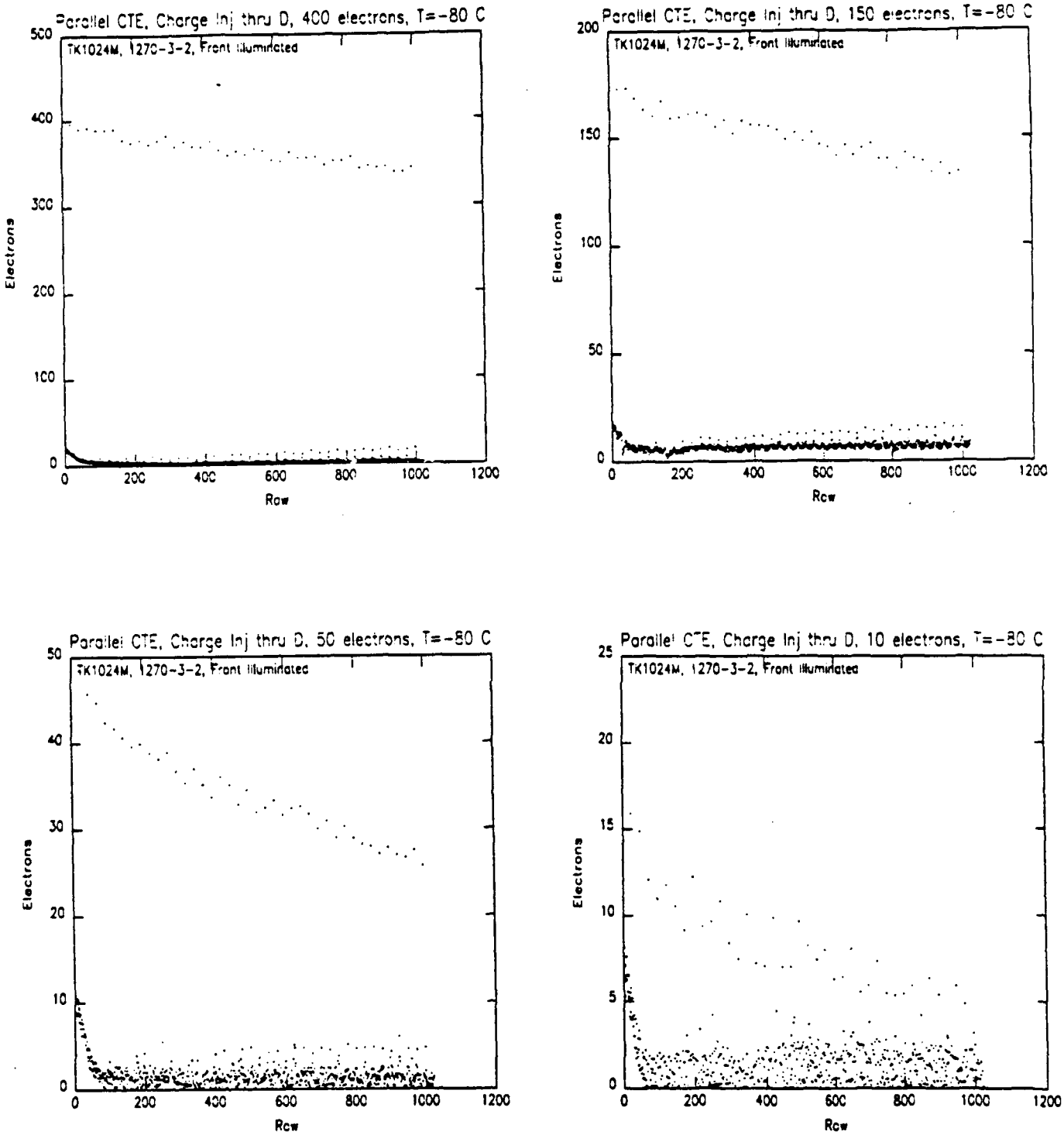
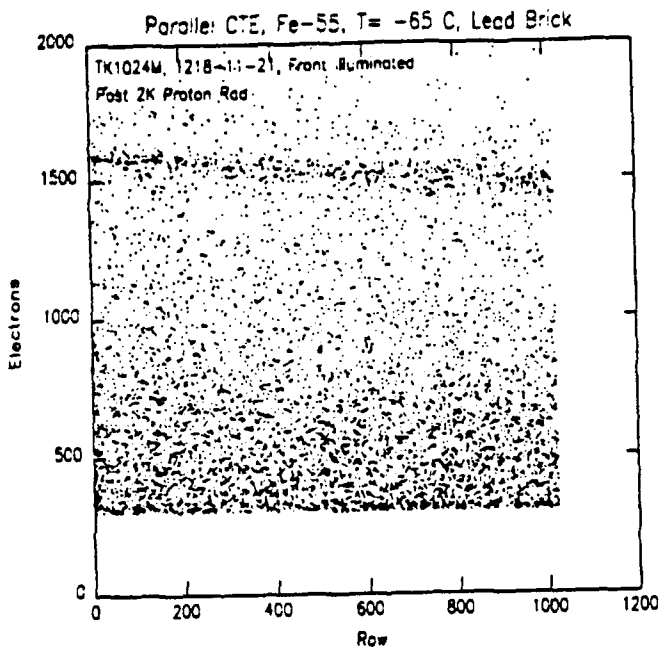
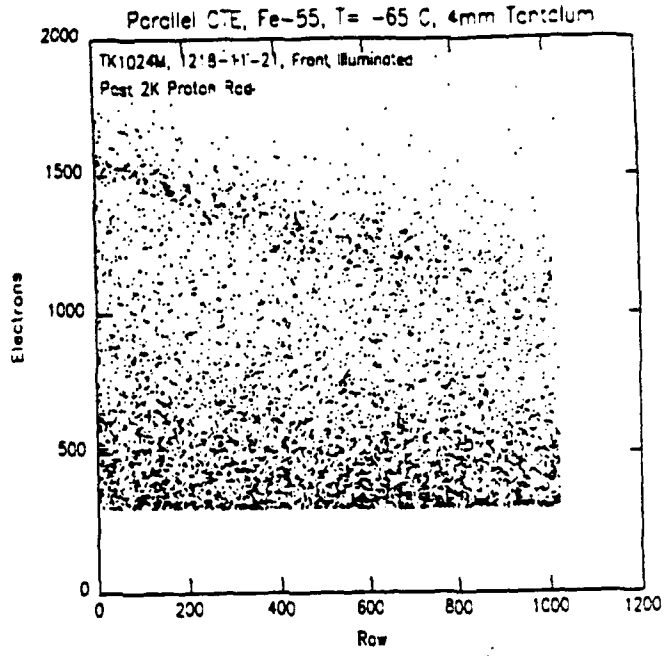


Figure 9: Charge injection through D amplifier with readout through C at 400, 150, 50, and 10 electron levels, $CTE(400) = \left(\frac{400-56}{400}\right)^{\frac{1}{1024}} = 0.999853$, $CTE(150) = 0.999697$, $CTE(50) = 0.999494$, $CTE(10) = 0.999245$





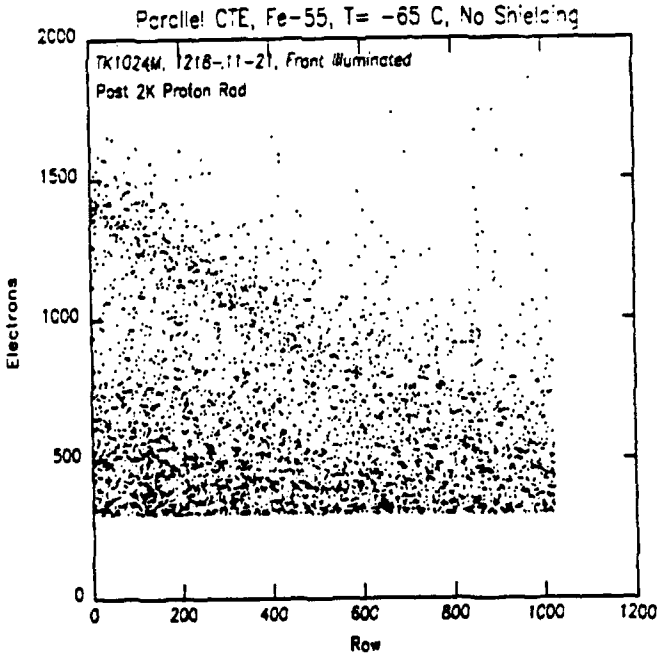


Figure 10: Fe^{55} x-ray response for device radiated with 2 Krads protons, CTE(lead) = 0.999938, CTE(4mm) = 0.999657, CTE(none) = 0.999063

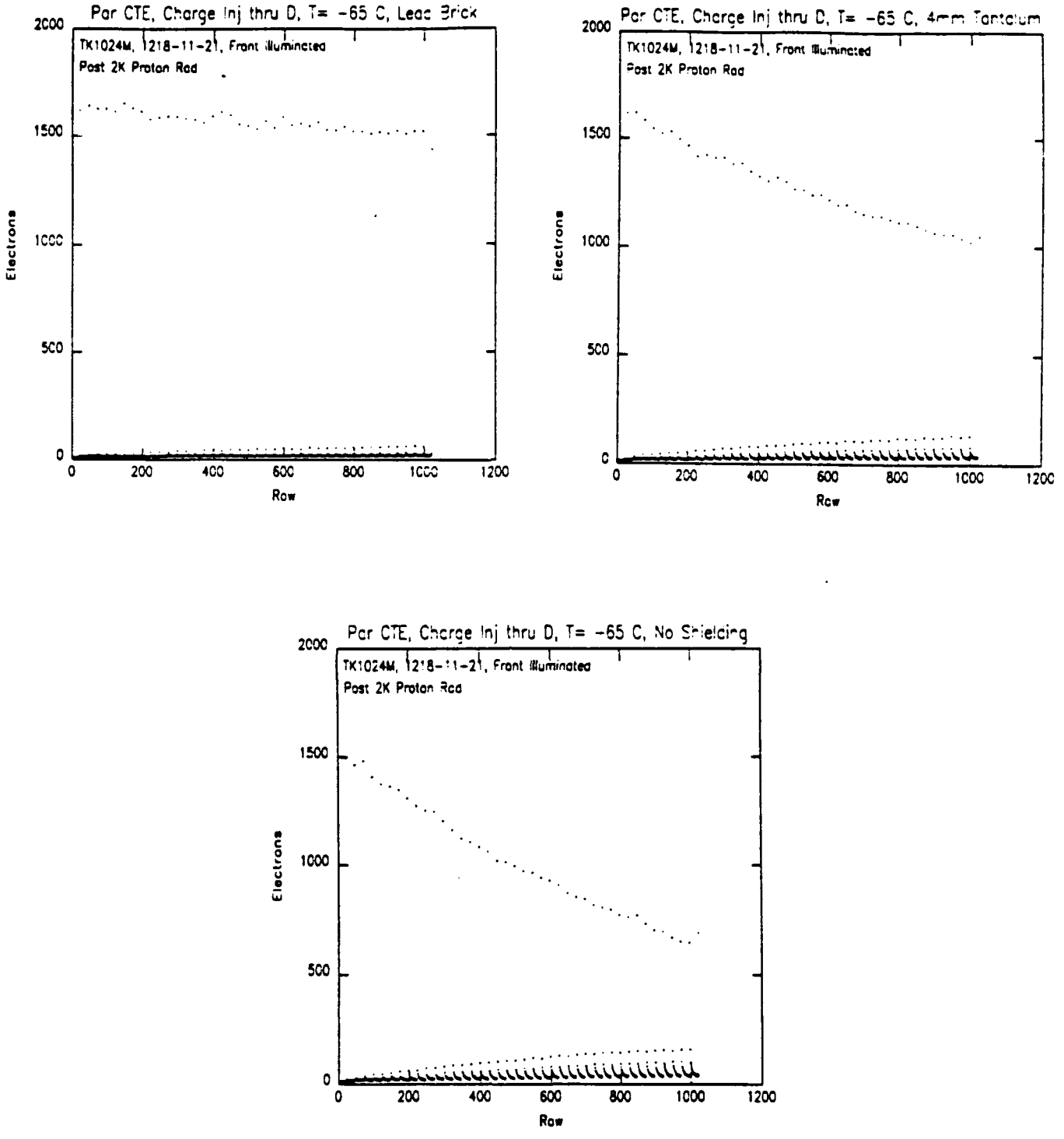


Figure 11: Charge injection response for device radiated with 2 Krads protons, CTE(lead) = 0.999931, CTE(4mm) = 0.999558, CTE(none) = 0.999180

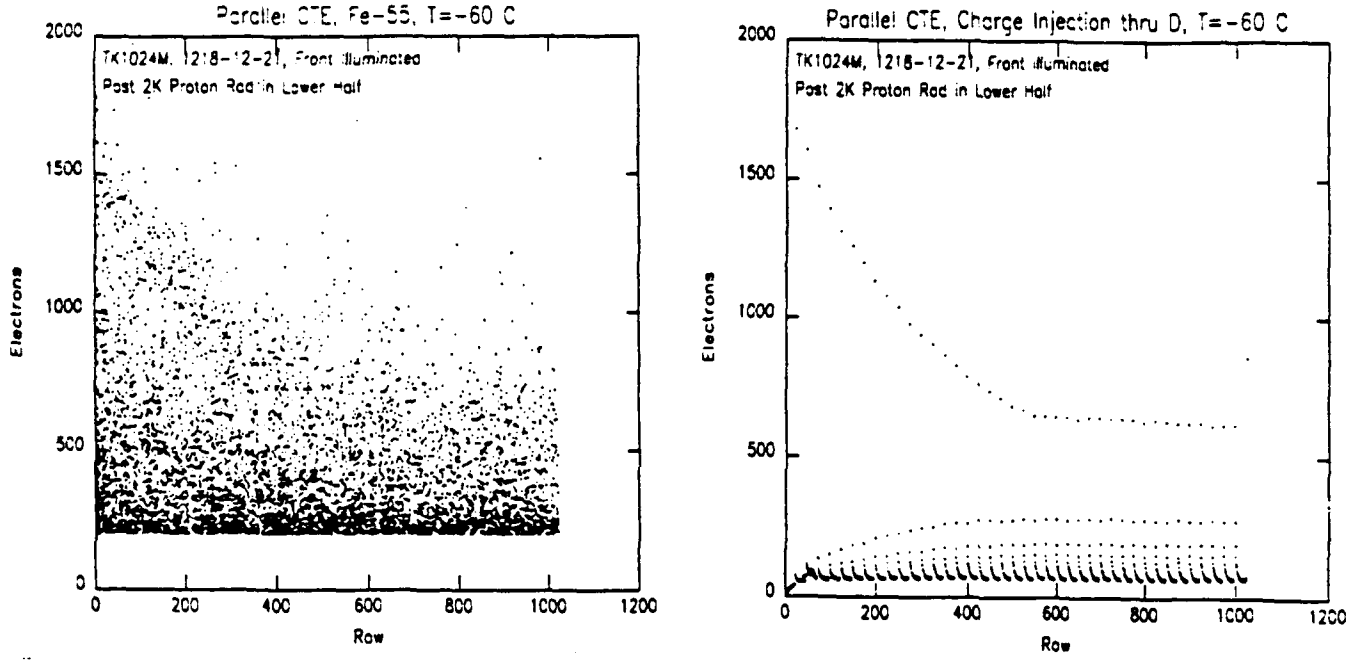


Figure 12: Fe^{55} x-ray response and charge injection through D amplifier with readout through C, device radiated with protons in lower half (approximately rows 1-512)